Title of the Experiment :

Analysis of Full Adder using eSim.

Theory :

The full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry. When a full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.

A full adder circuit can be implemented with the help of two half adder circuits. Thefirst will have the half adder to add A and B to produce a partial Sum. The second half adder logic can be used to add input carry to the Sum produced by the first half adder to get the final sum output. If any of the half adder logic produces a carry, there will be an output carry.

Schematic Diagram :

The circuit schematic of full adder in eSim is as shown below:

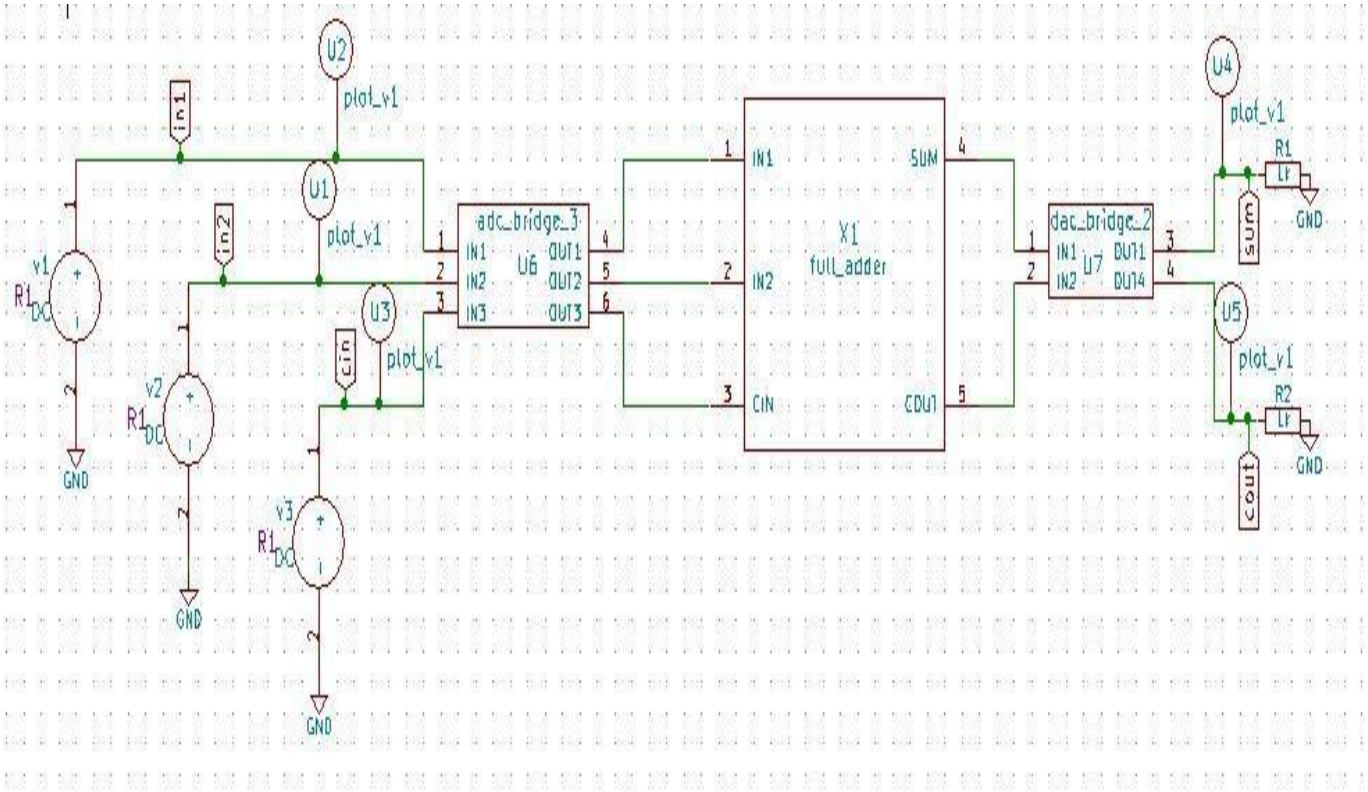

Figure 1: Full adder

Simulation Results :

1. Python plots:

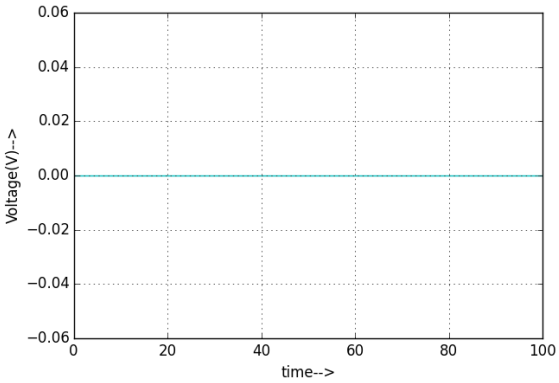

Figure 2: output Sum

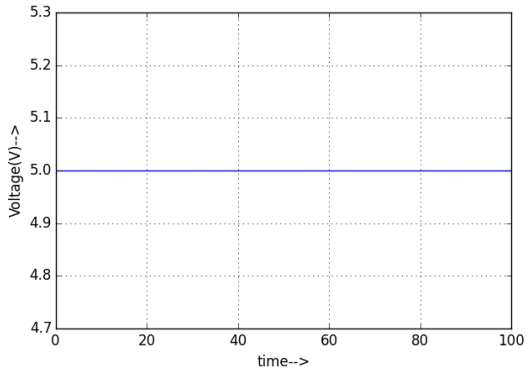

Figure 3: output Carry

2. Ngspice plots:

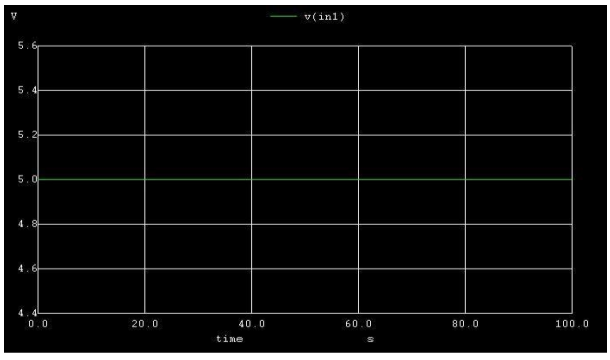

Figure 4: Ngspice Input-1 Plot

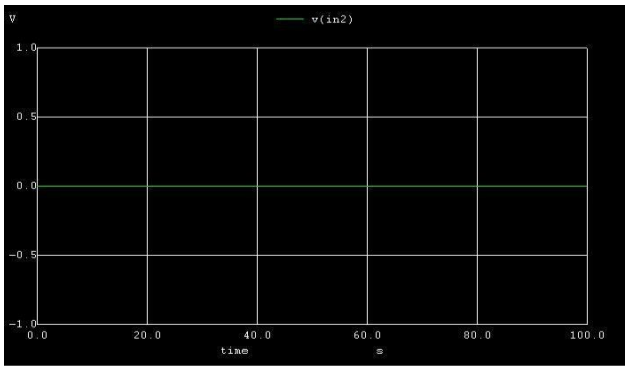

Figure 5: Ngspice Input-2 Plot

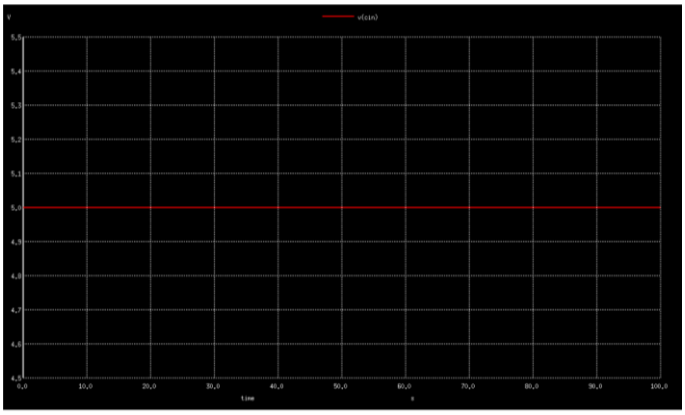

Figure 6: Ngspice Input Cin Plot

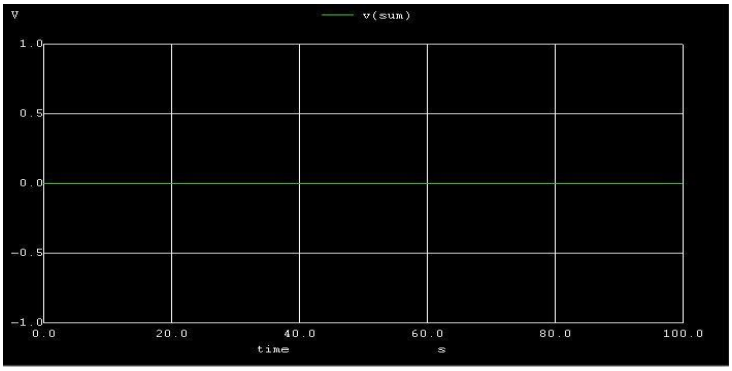

Figure 7: Ngspice Output Sum Plot

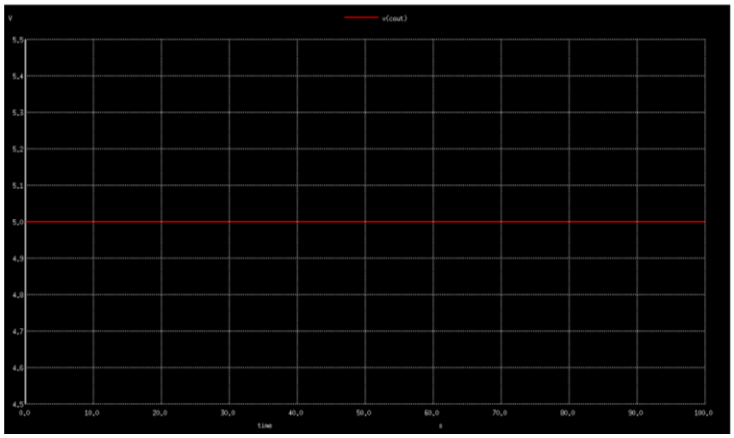

Figure 8: Ngspice Output Carry Plot

Reference:

[1]https://www.electronicshub.org/half-adder-and-full-adder-circuits/ referred on 16/07/2017.