Title :- 2 BIT LOGIC UNIT

Theory :-

Logic micro operations specify binary operations for strings of bits stored in registers. These operations consider each bit of registers separately and treat them as binary variables. Figure 1 shows one stage of a circuit that generates the four basic logic micro operations. It consists of 4 gates and a multiplexer each of the four logic operations is generated through a gate that performs the required logic. The outputs of the gates are applied to the data inputs of the multiplexer. The two selection inputs S1 and S0 choose one of the data inputs of the multiplexers and direct it values to the output.

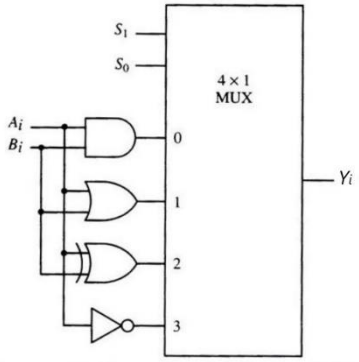


Figure 1: Schematic of 1-bit Logic Unit

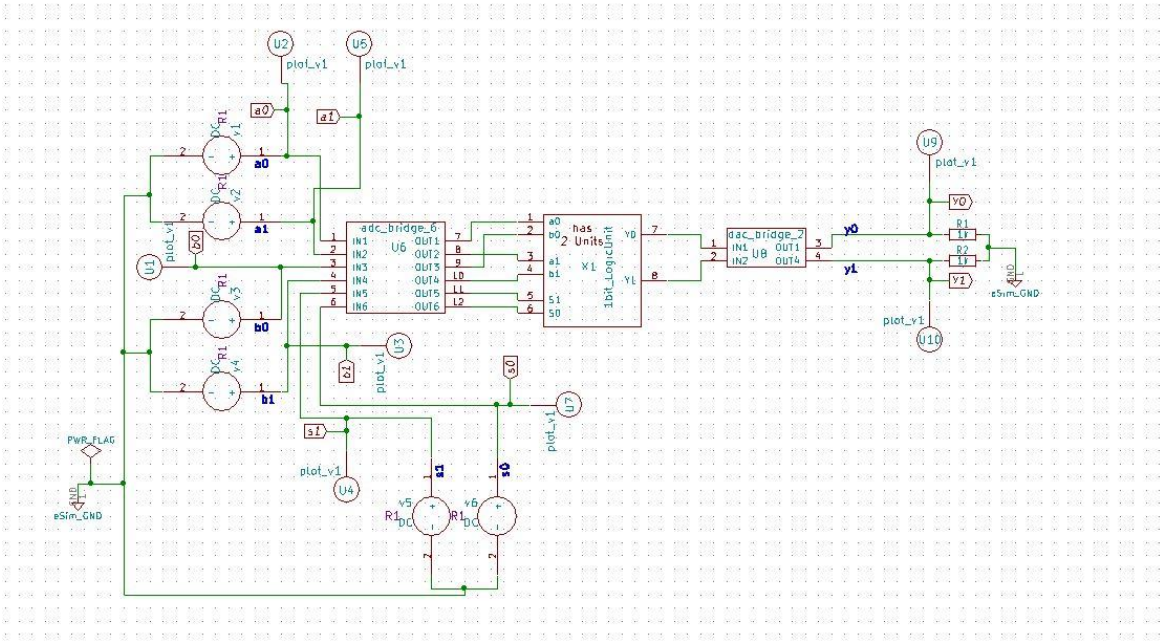
Here in this logical block consists of two sets of such gates i.e. it performs operations on two bits (a0,b0) and (a1,b1) . Then one operation is selected through a dual 4 : 1 Multiplexer by the select inputs s0 and s1 generating outputs y0,y1 corresponding to bits (a0,b0) and (a1,b1).

Function Table:-

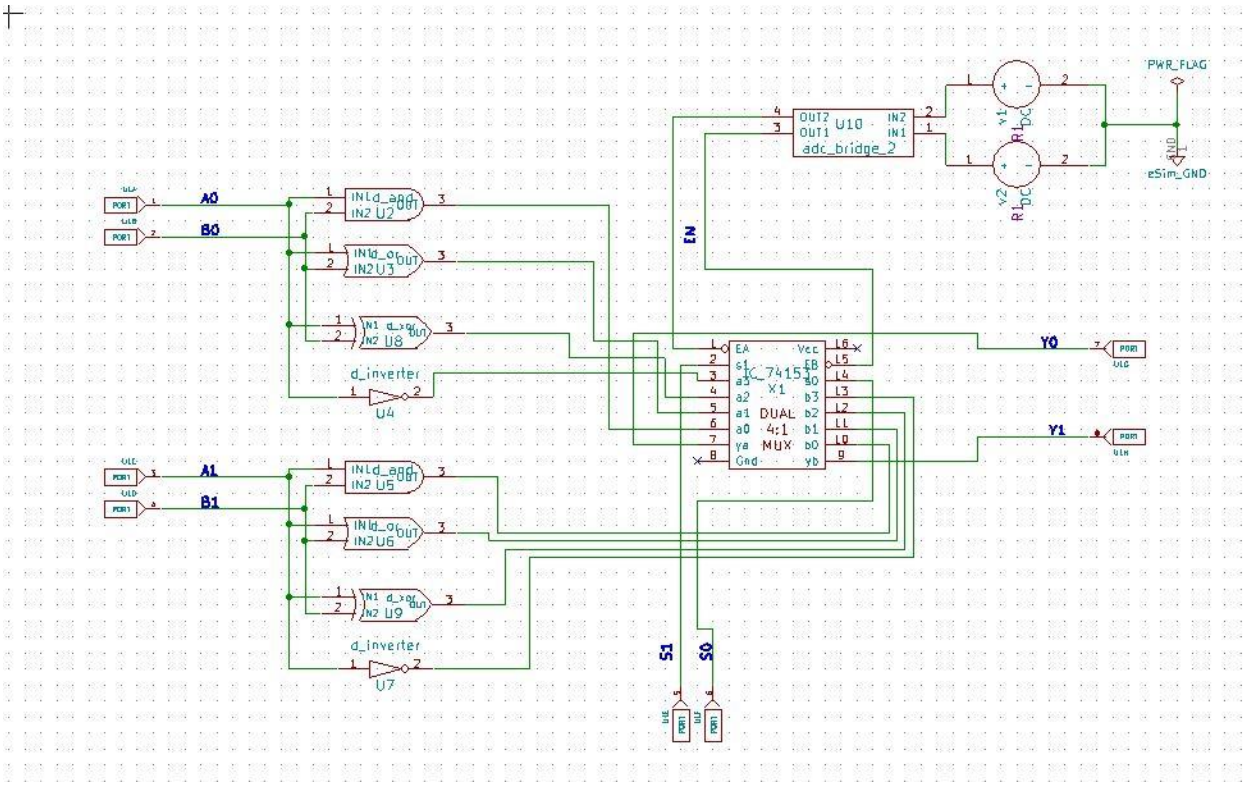
S1	S0	Y0	Y1
0	0	a0 AND b0	a1 AND b1
0	1	a0 OR b0	a1 OR b1
1	0	a0 XOR b0	a1 XOR b1
1	1	NOT a0	NOT b0

Schematic Diagram :-

Circuit for logical operation on 2 bits:



Subcircuit Schematic for 1bit_LogicalUnit:-



Simulation Results :-

Input:-

a[1:0] - 1 0

b[1:0] - 1 1

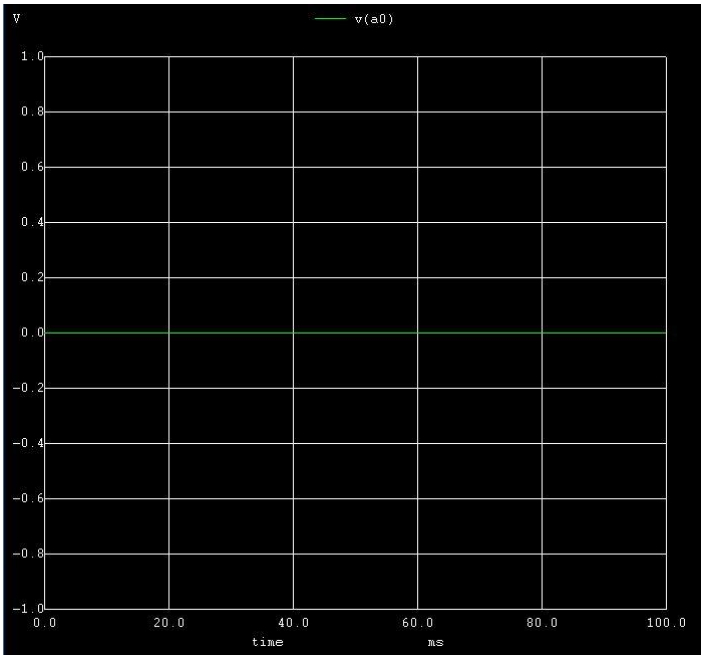
Output:-

S1	S0	Logic Operation	Y1	Y0
0	0	AND	1	0
0	1	OR	1	1
1	0	XOR	0	1
1	1	NOT	0	1

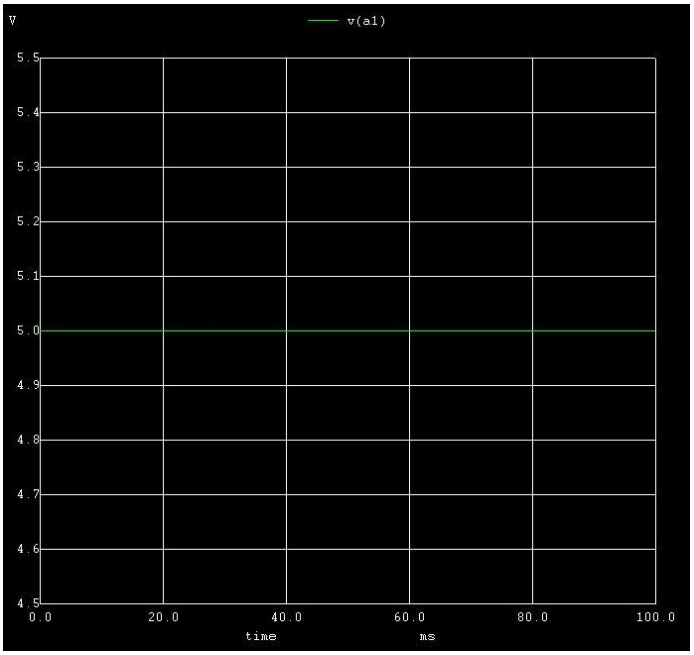
NGSPICE PLOTS

Input:-

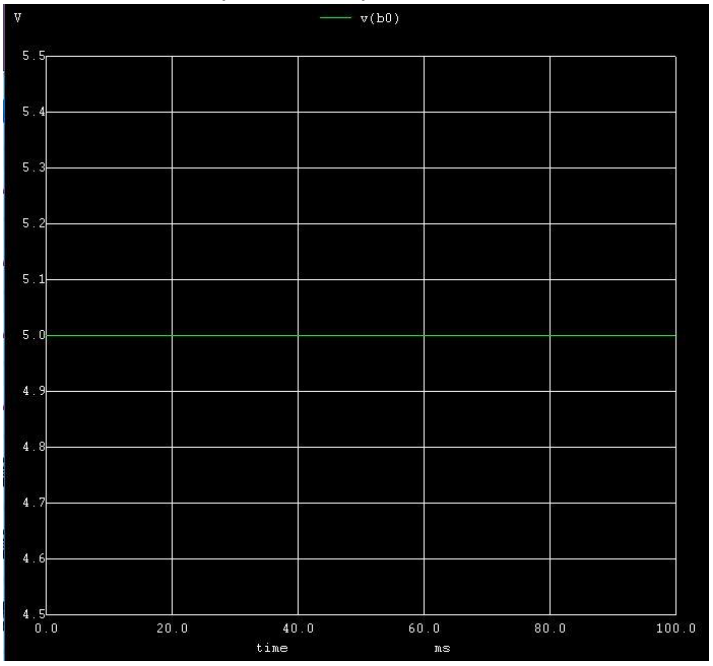
a0 (V1= 0v)



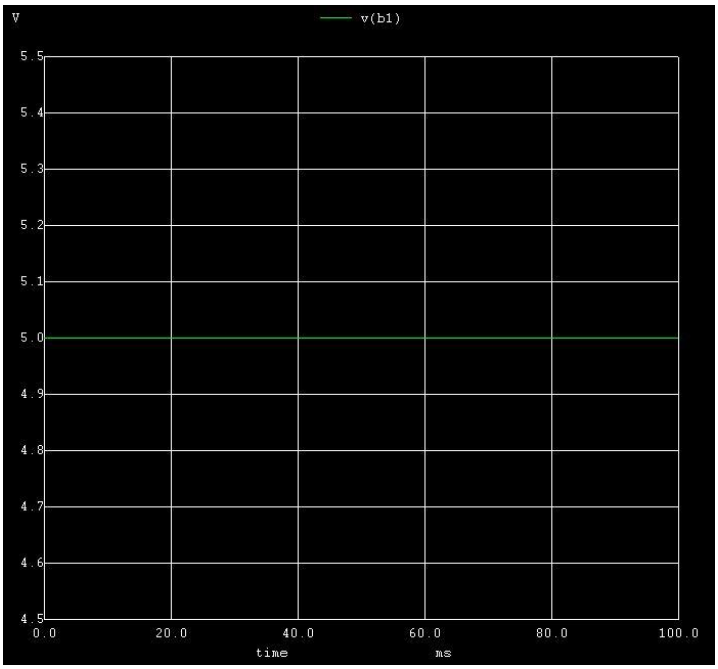
a1 (v2= 5v)



b0 (v3 = 5 v)

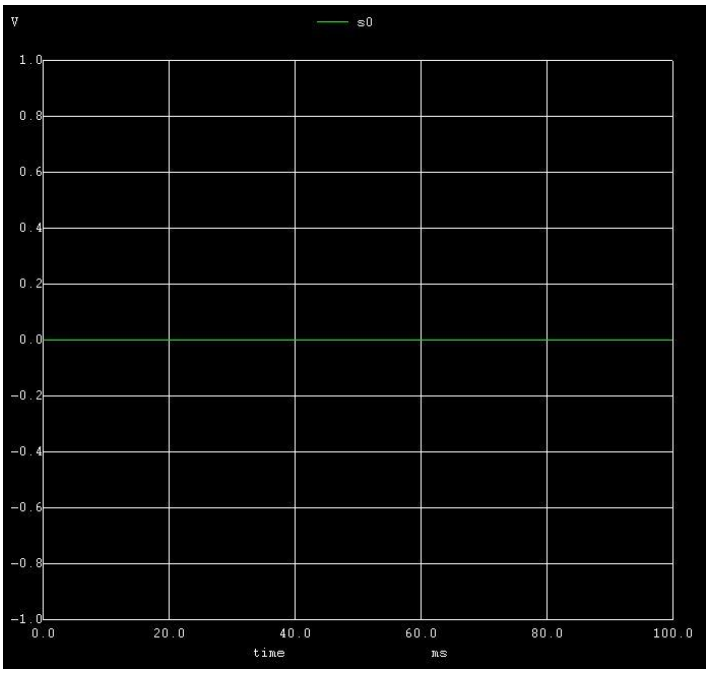


b1 (v4= 5v)

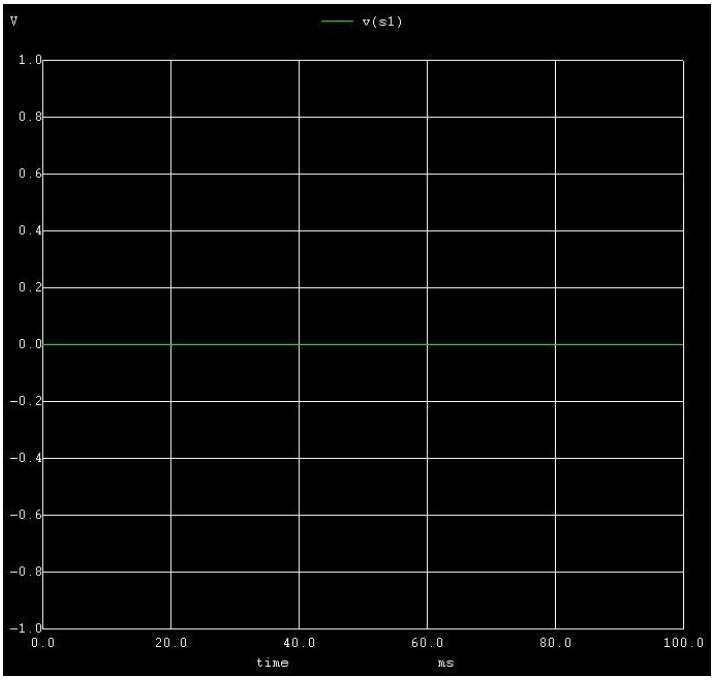


Output when s0 = ‘ 0 ‘ and s1 = ‘ 0 ‘

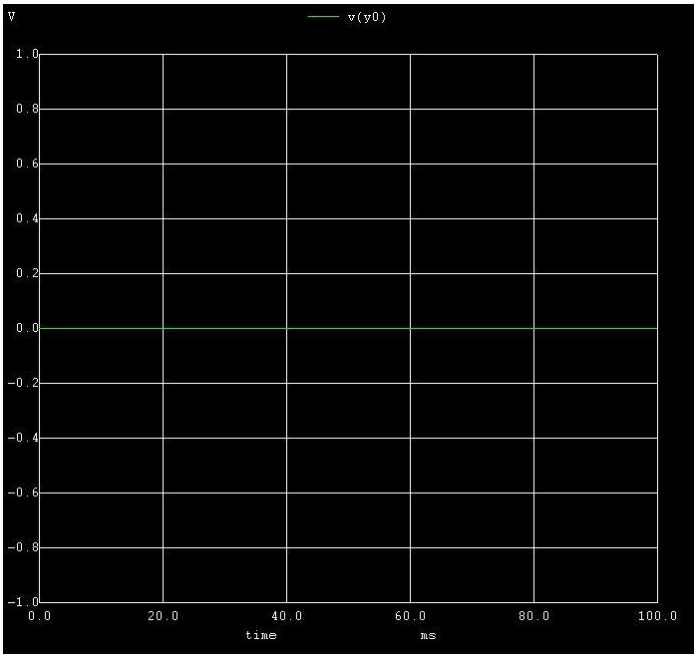
s0 (v6 = 0v)



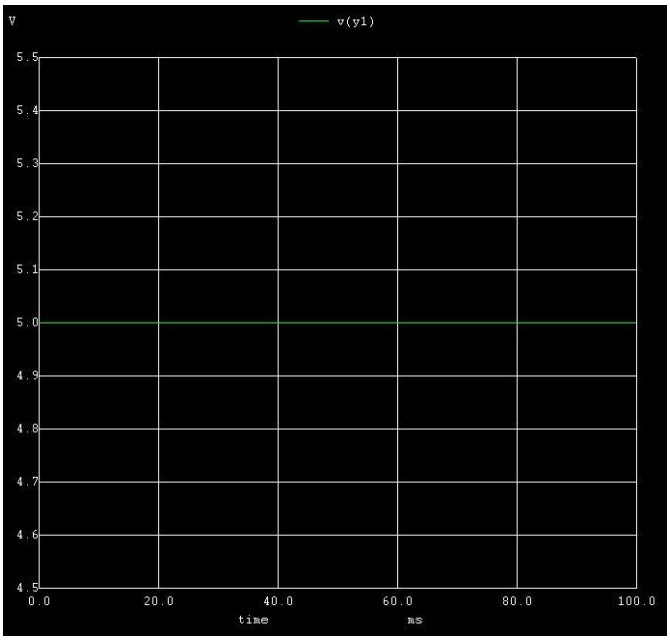
s1 (v5= 0v)



y0

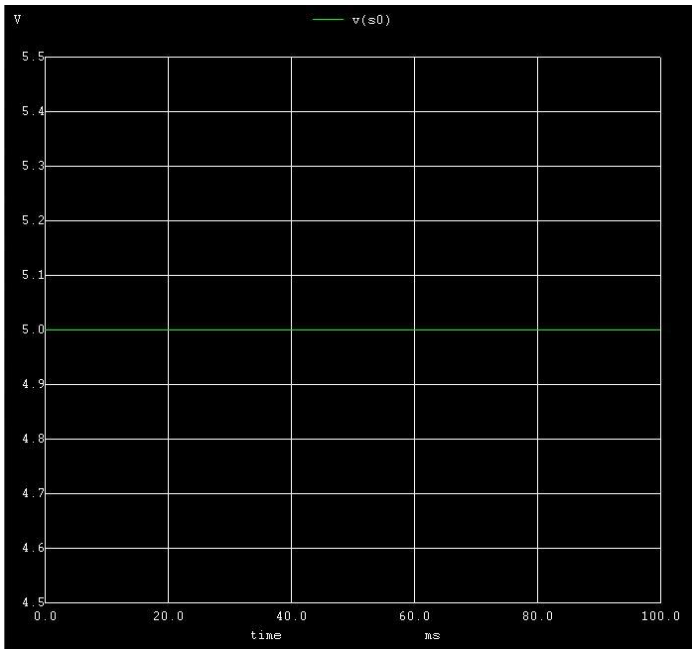


y1

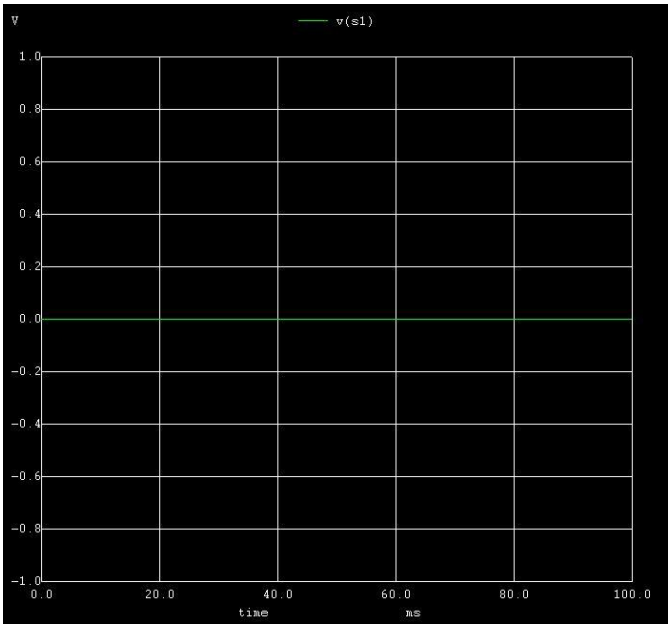


Output when s0 = ‘ 1 ‘ and s1 = ‘ 0 ‘

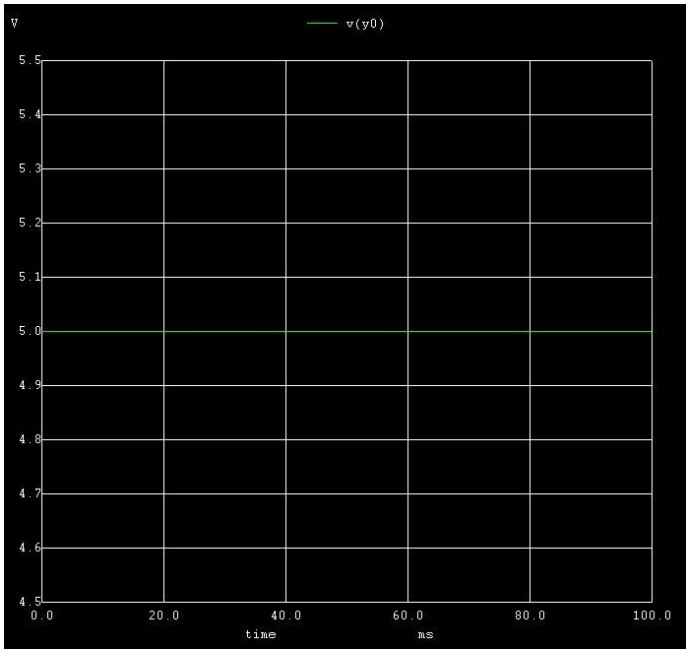
s0 (v6 = 5v)



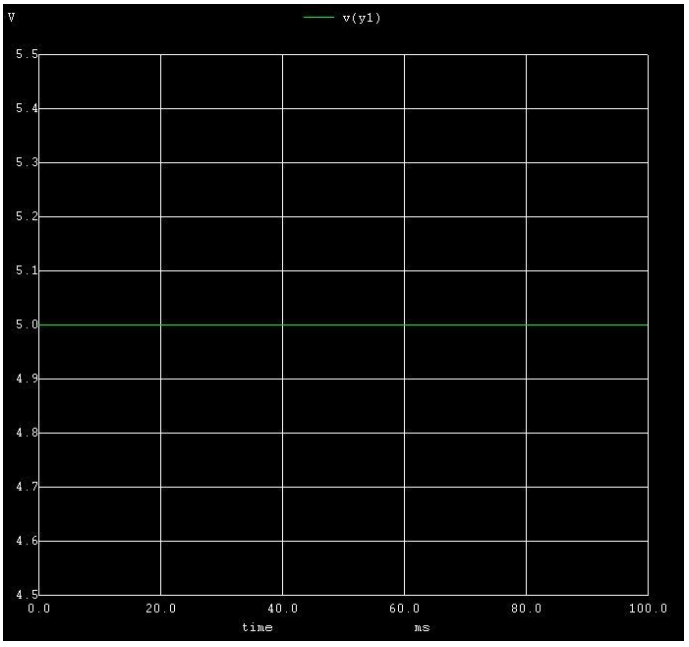
s1 (v5= 0v)



y0

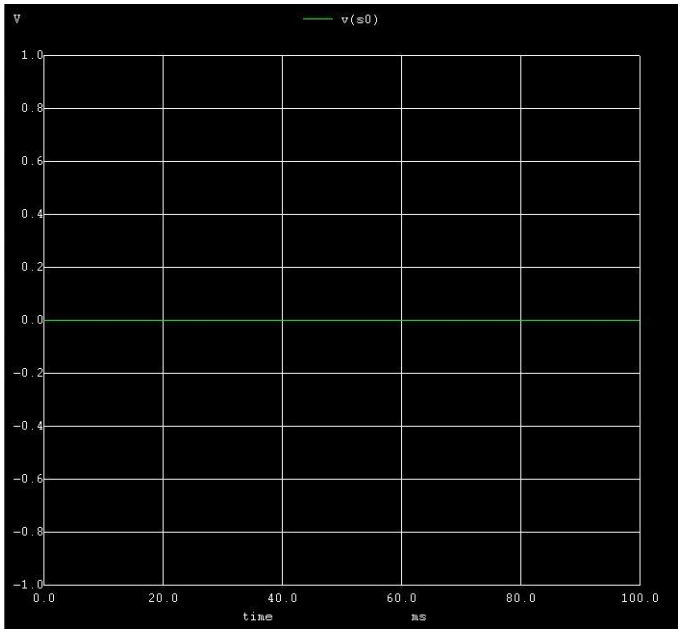


y1

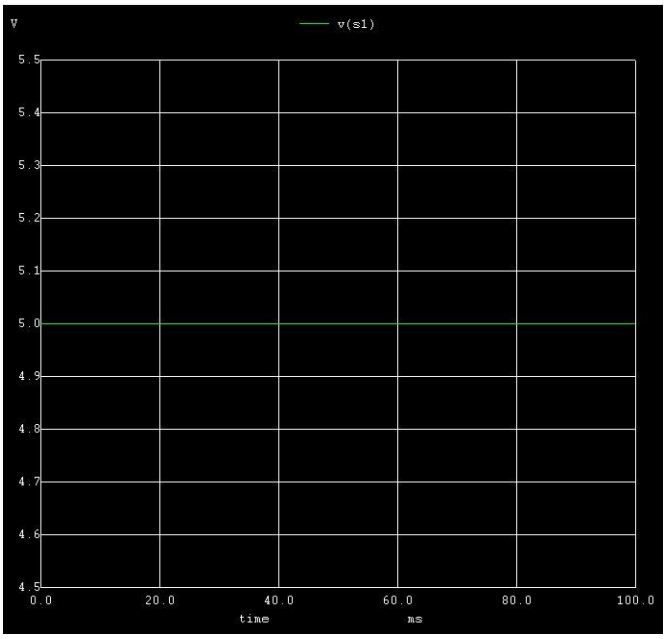


Output when s0 = ‘ 0 ‘ and s1 = ‘ 1 ‘

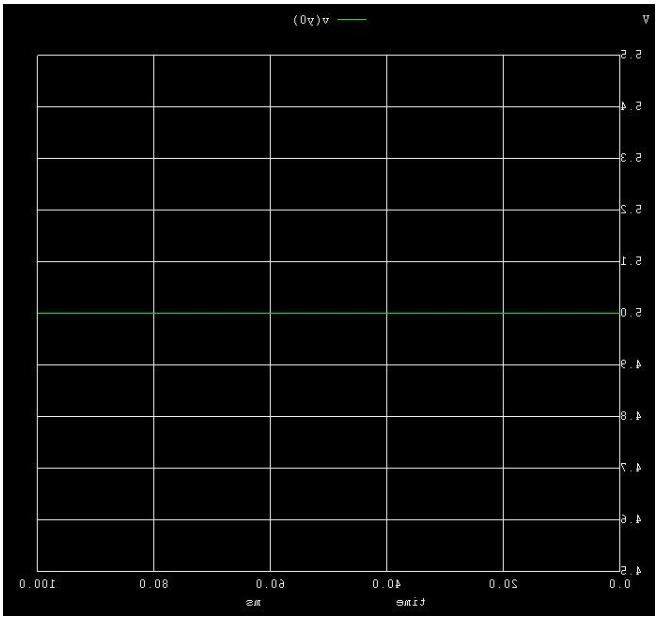
s0 (v6 = 0v)



s1 (v5 = 5v)



y0



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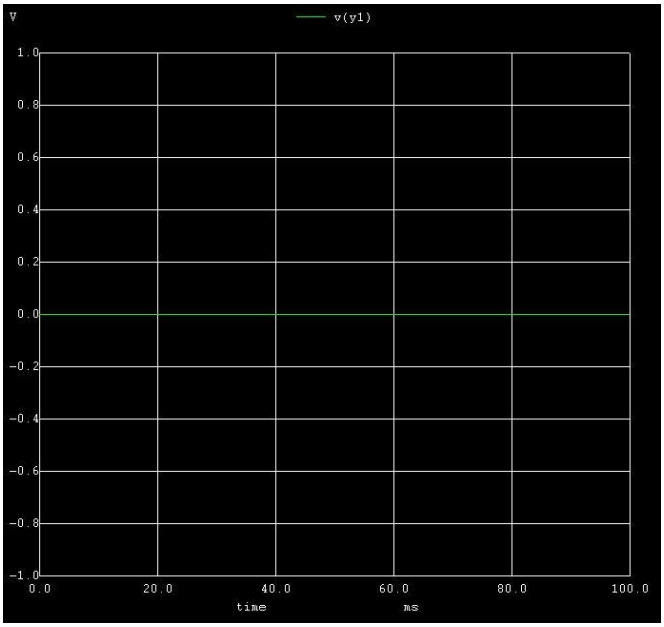
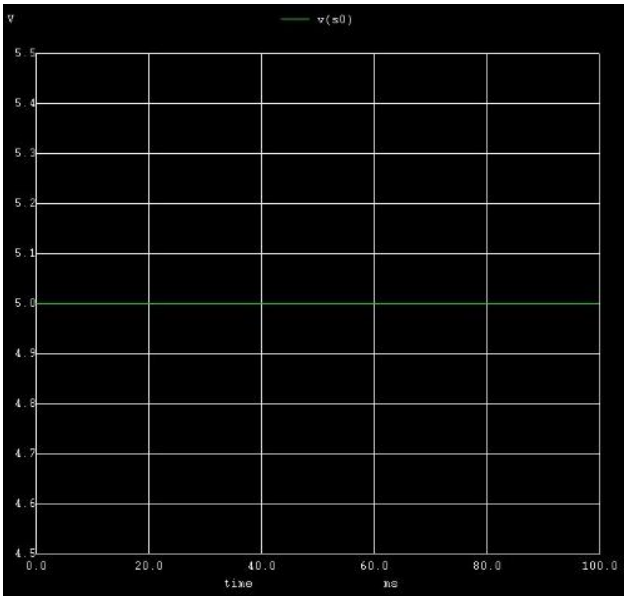
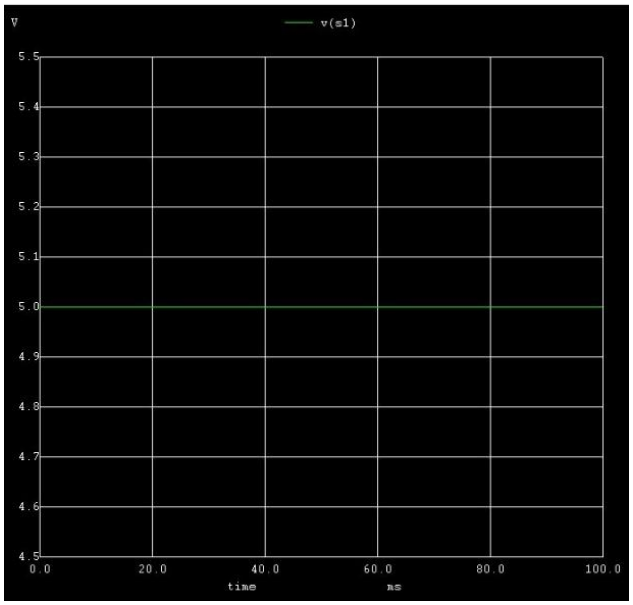


Output when s0 = ‘ 1 ‘ and s1 = ‘ 1 ‘

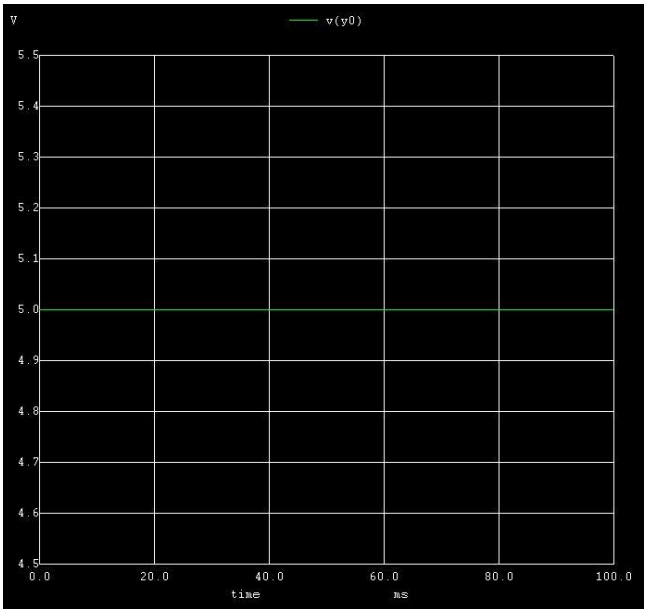
s0 (v6 = 5v)



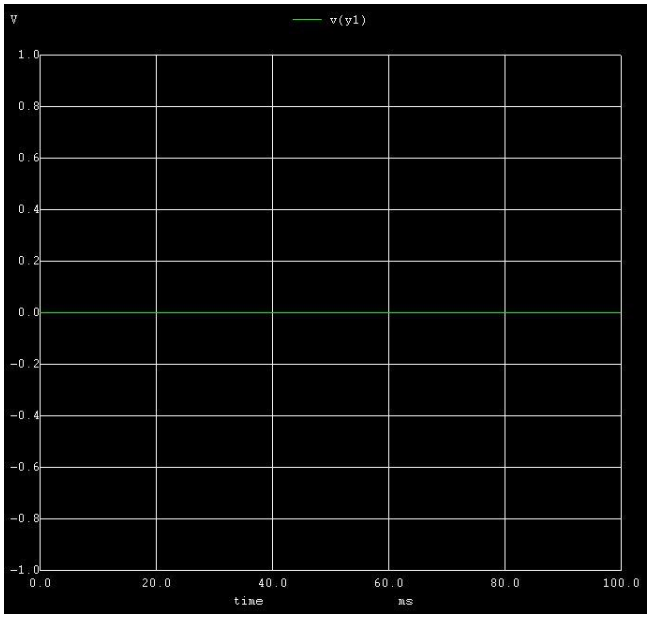
s1 (v5 = 5v)



y0



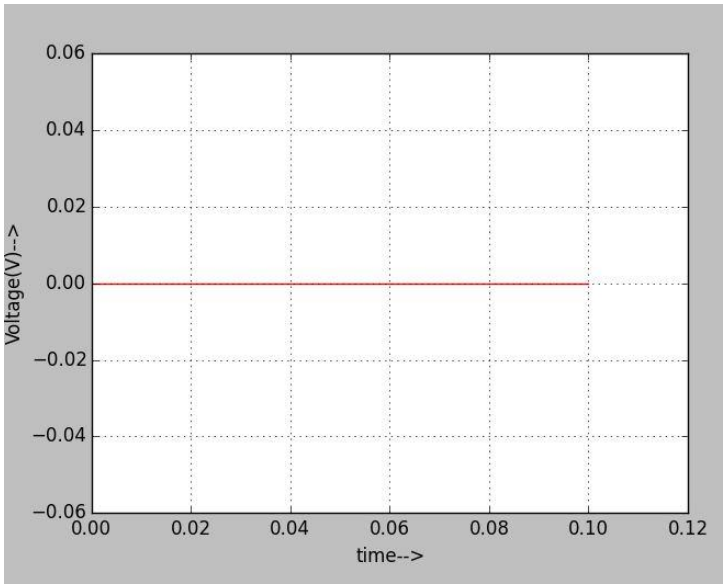
y1



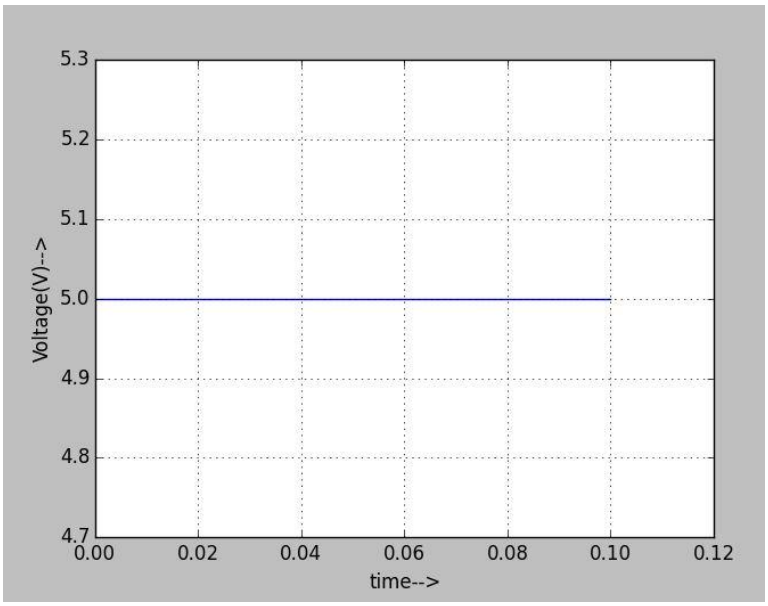
PYTHON PLOTS:-

Input:-

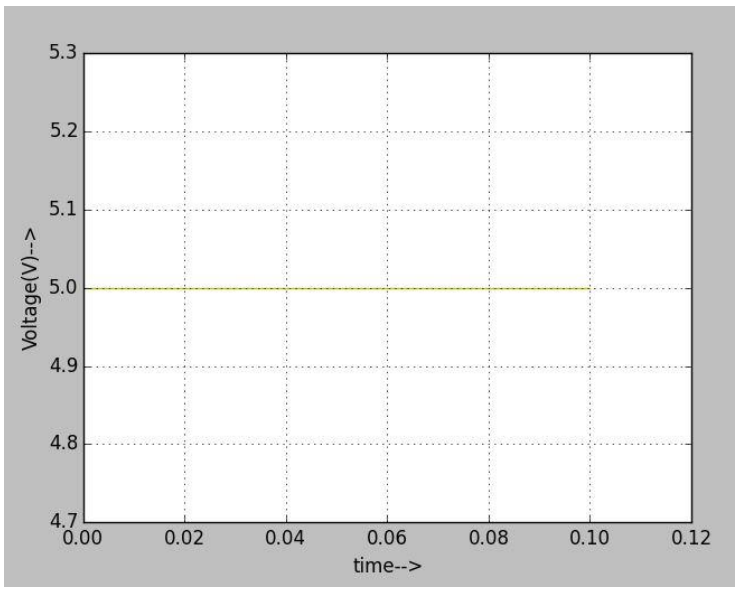
a0 (V1= 0v)



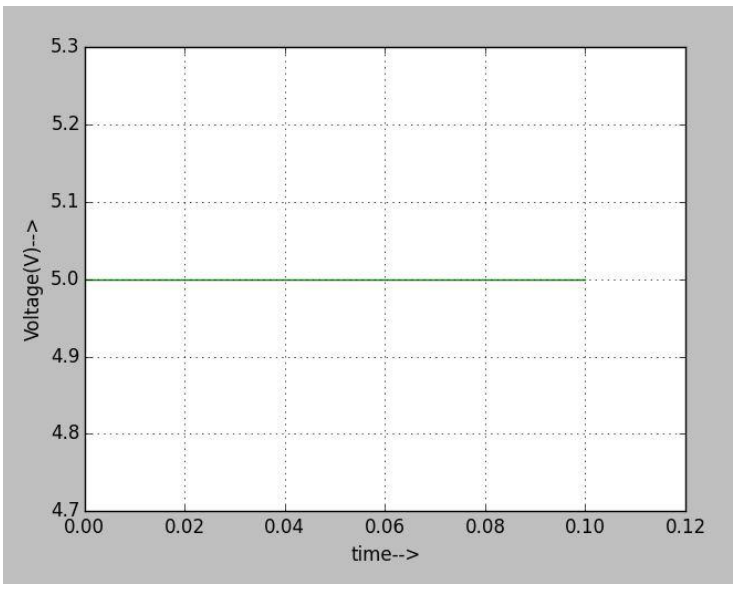
a1 (v2= 5v)



b0 (v3 = 5 v)

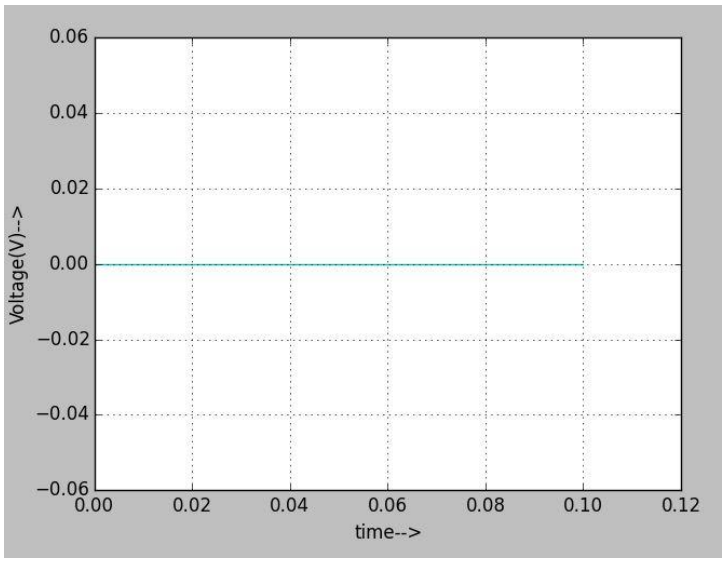


b1 (v4= 5v)

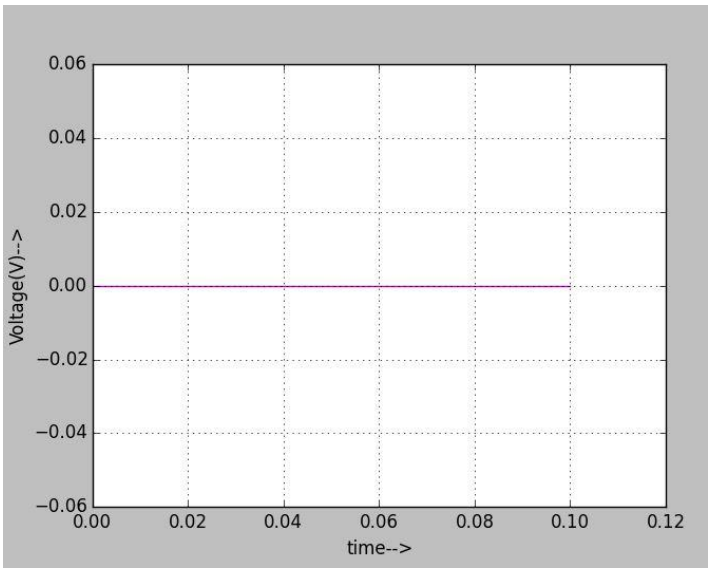


Output when s0 = ‘ 0 ‘ and s1 = ‘ 0 ‘

s0 (v6 = 0 v)



s1 (v5 = 0 v)



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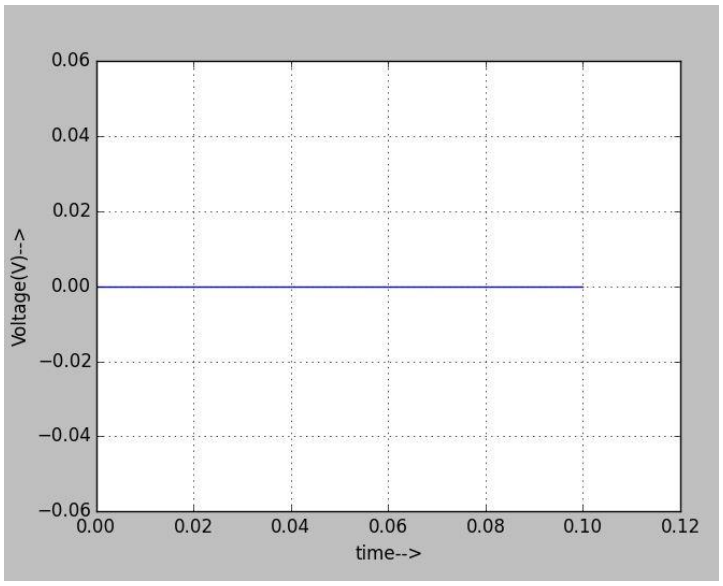

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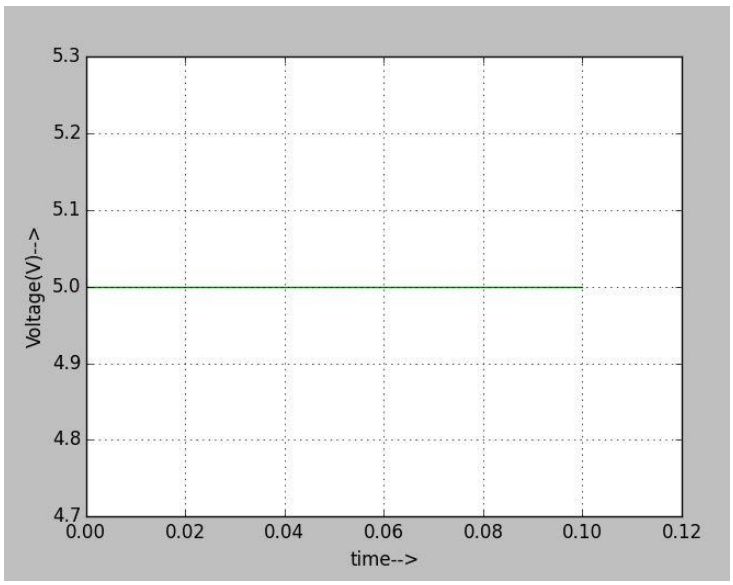
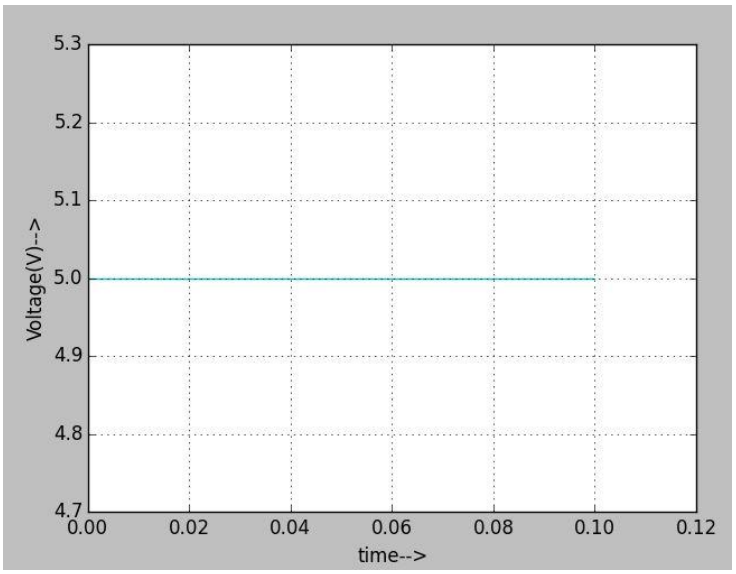
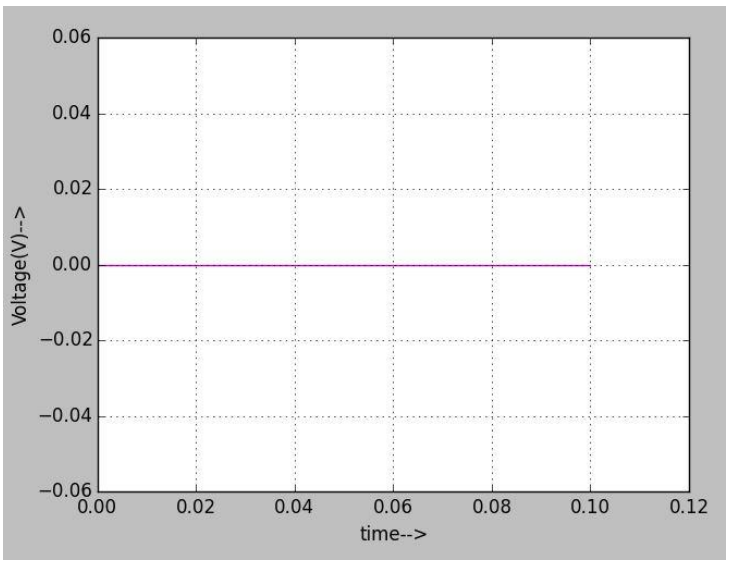


Output when s0 = ‘ 1 ‘ and s1 = ‘ 0 ‘

s0 (v6 = 5 v)



s1 (v5 = 0 v)



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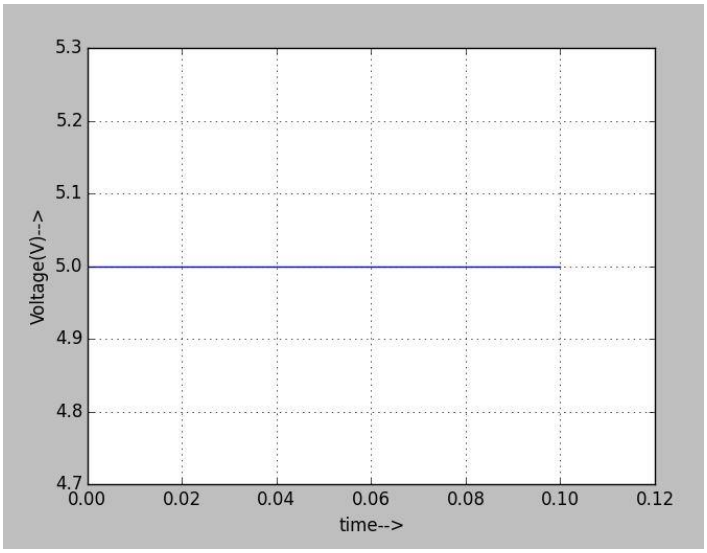

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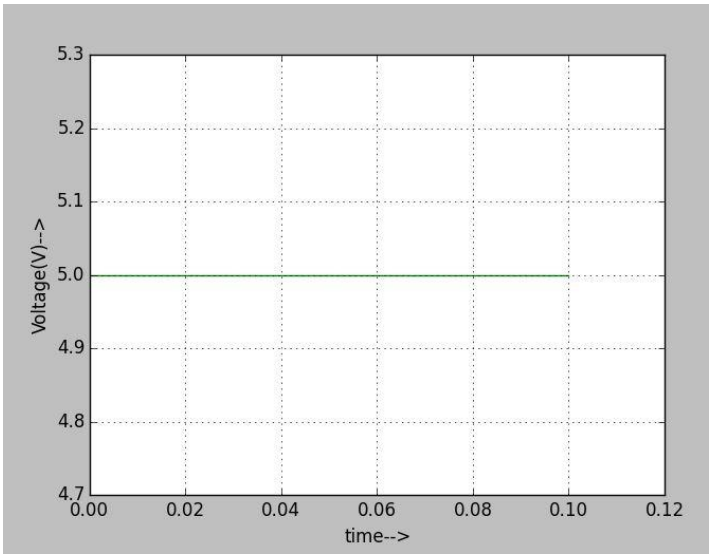
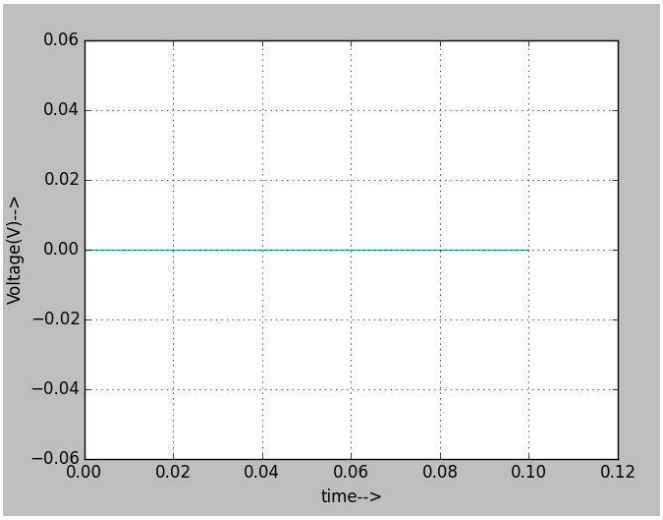
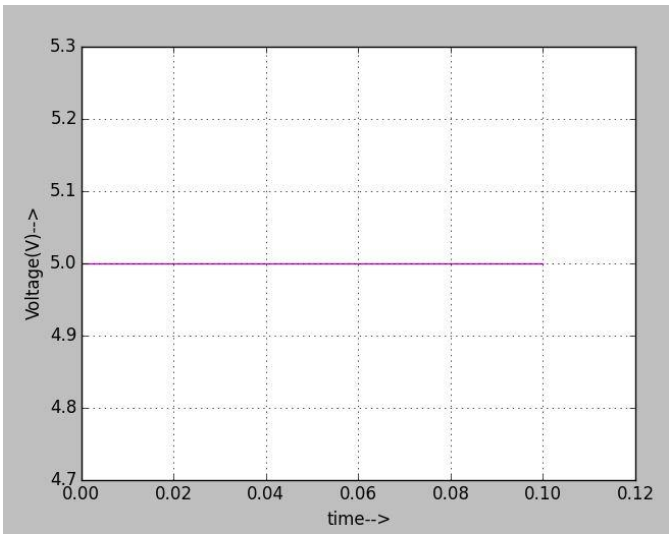


Output when s0 = ‘ 0 ‘ and s1 = ‘ 1 ‘

s0 (v6 = 0v)



s1 (v5 = 5v)



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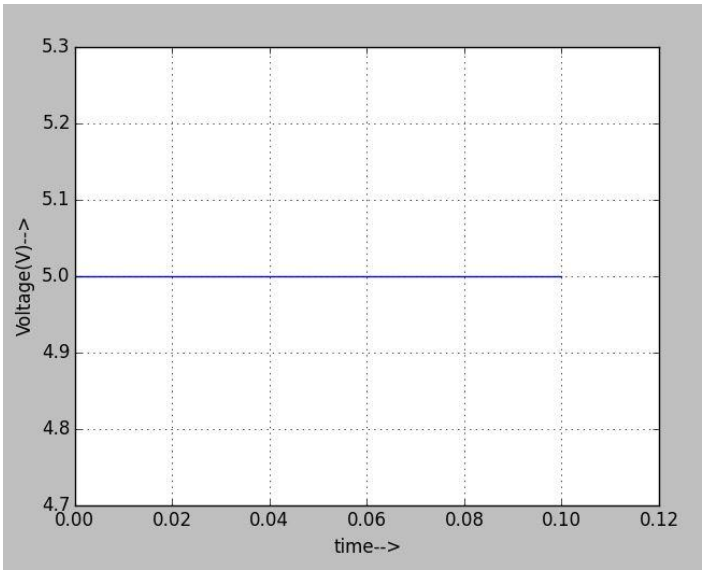

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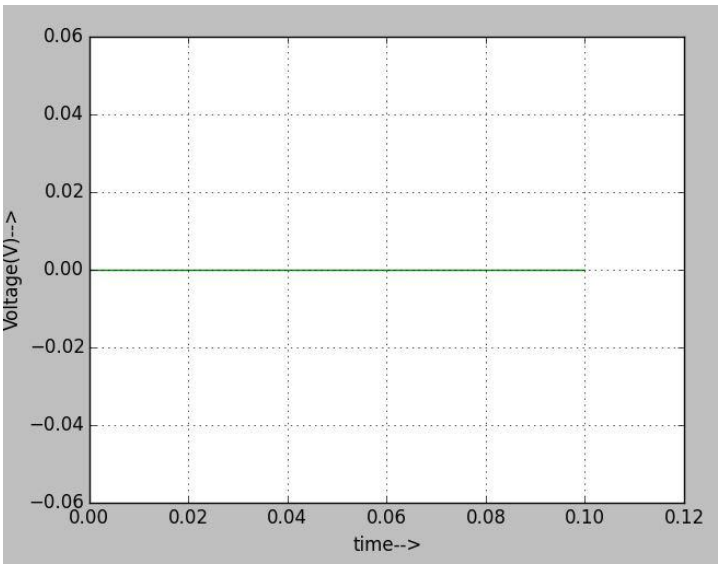
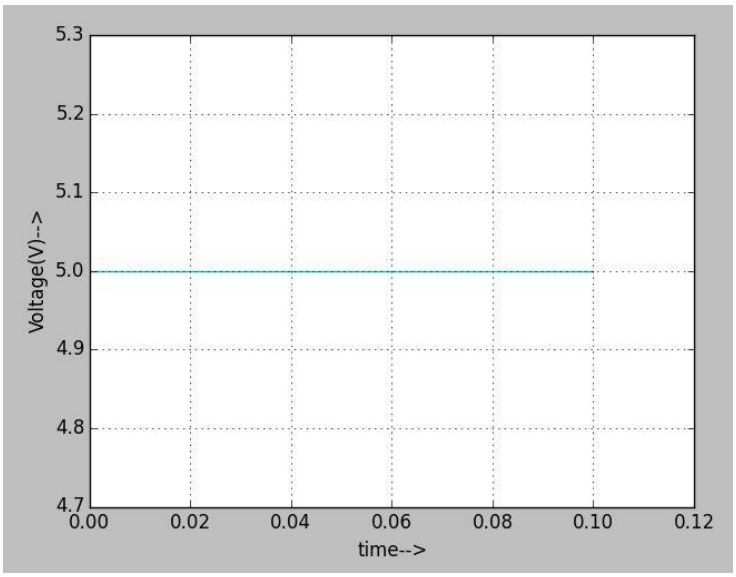
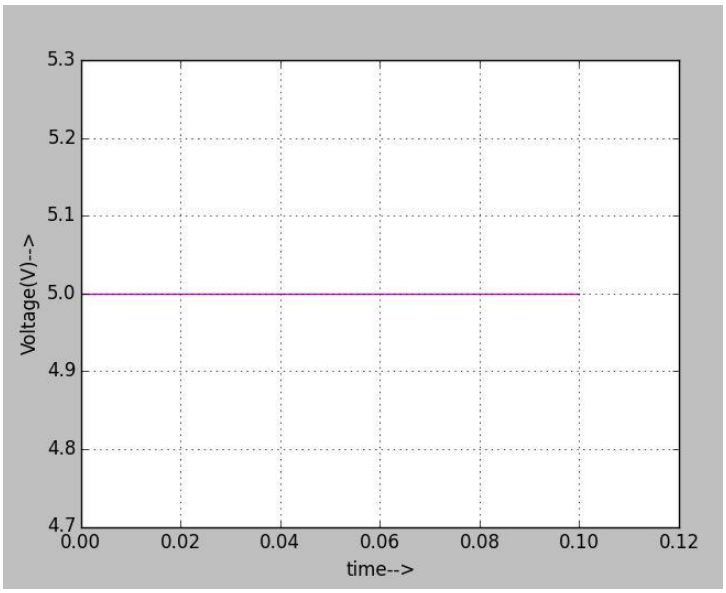


Output when s0 = ‘ 1 ‘ and s1 = ‘ 1 ‘

s0 (v6 = 5 v)



s1 (v5 = 5 v)



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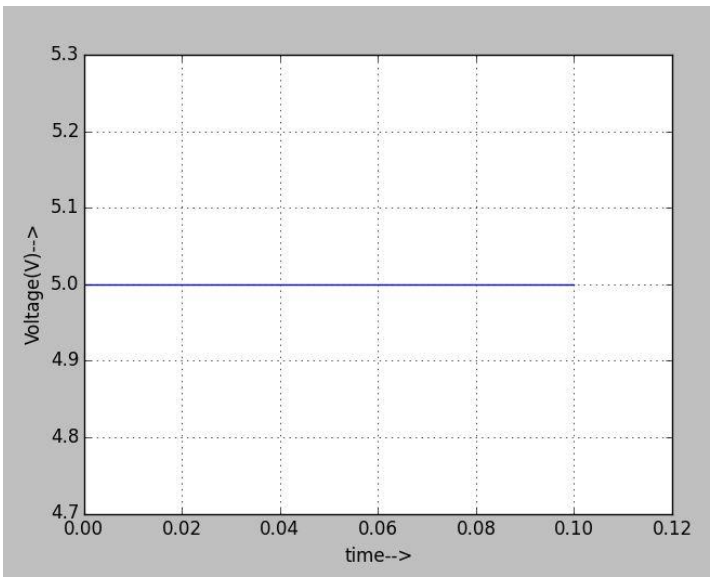

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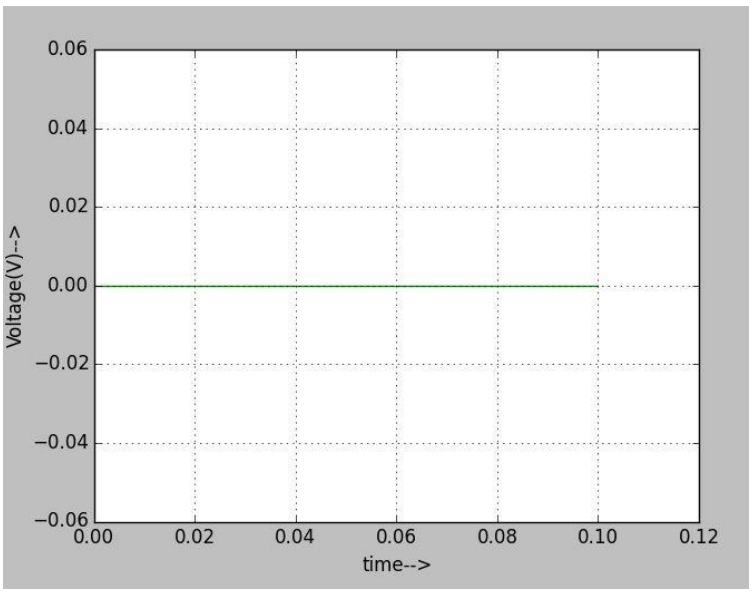

References:-

1) https://pdfs.semanticscholar.org/16ab/11d6142791a1366e69665849188839128598.pdf