TITLE OF THE EXPERIMENT

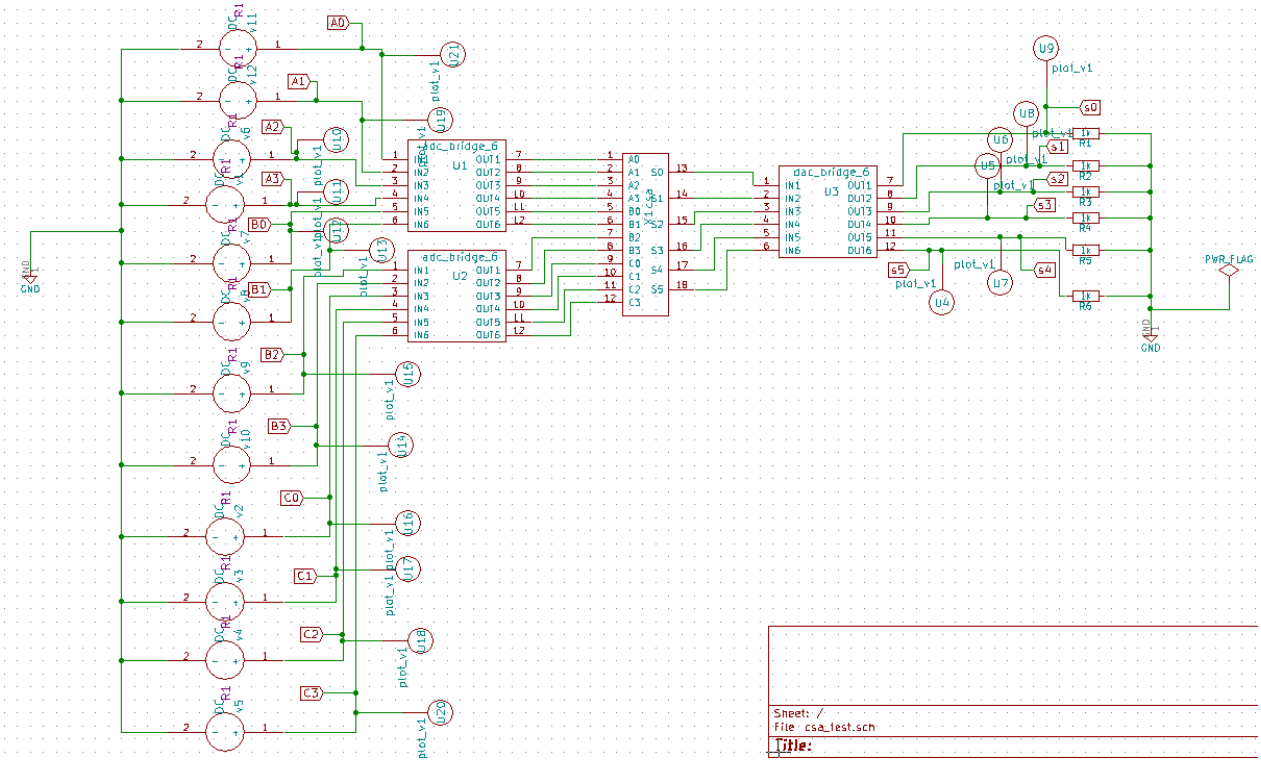
DESIGN OF FOUR BIT CARRY SAVE ADDER USING SUBCIRCUIT BUILDER

THEORY

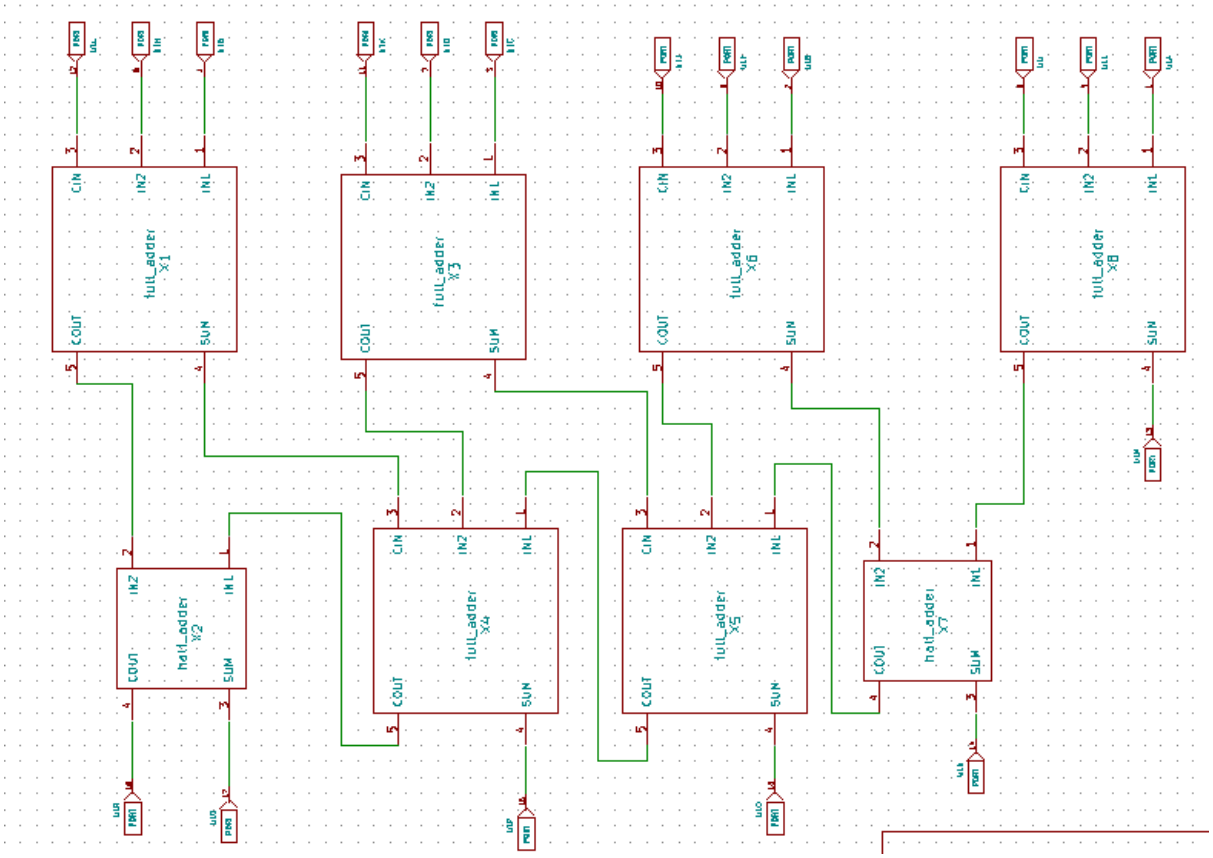
Carry save adder is a design of a high speed multioperand adder.A carry save adder consists of a ladder of stand alone full adders .The 4-bit CSA consists of 4 disjoint full adders where each of which computes a single sum and carry bit based on corresponding bits of the three input numbers.It consumes three 4 bit input integers to be added and produces two outputs partial sum and partial carry.This partial sum and carry are added after using half adder and full adder.

Schematic Diagram

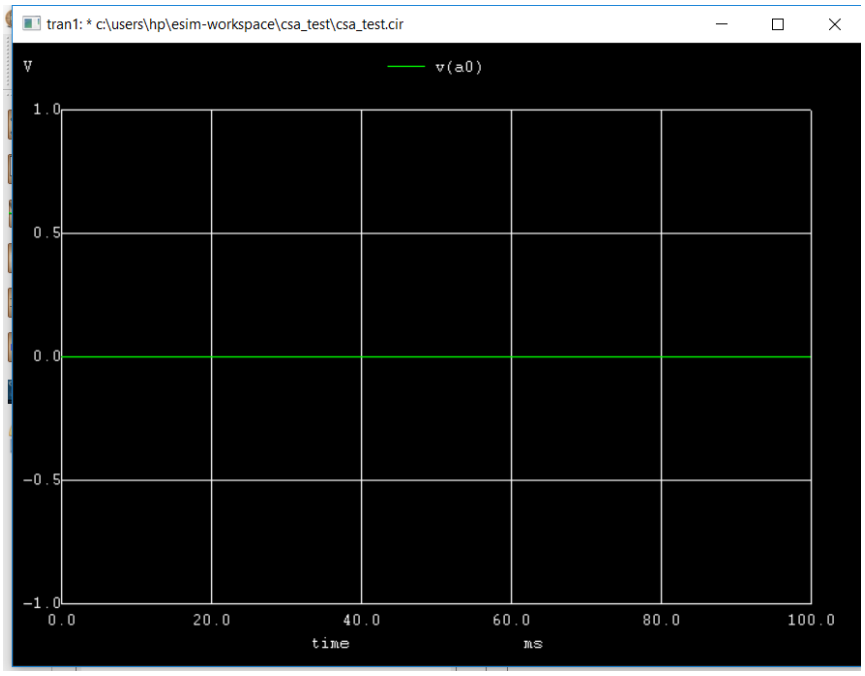
The schematic diagram of four bit carry save adder is.

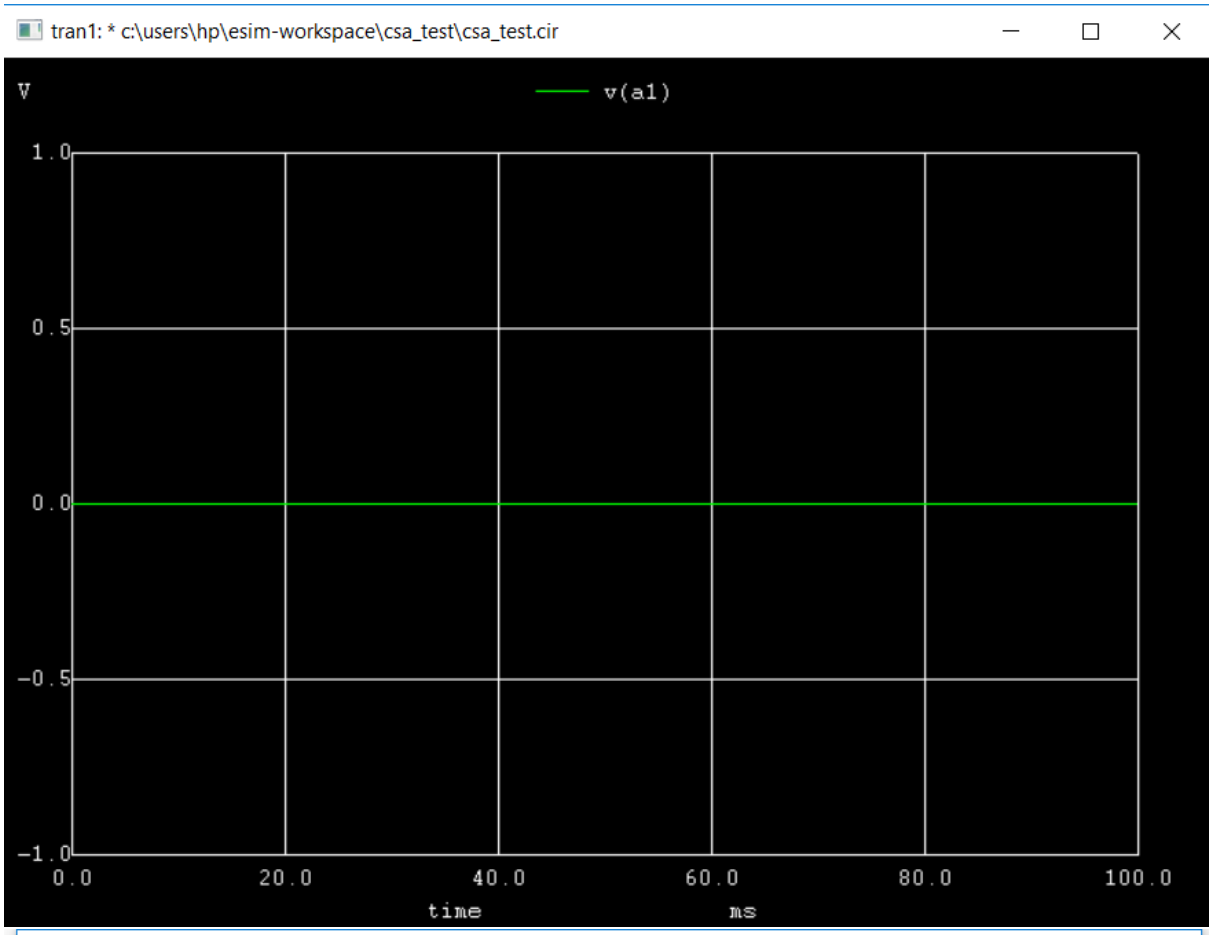


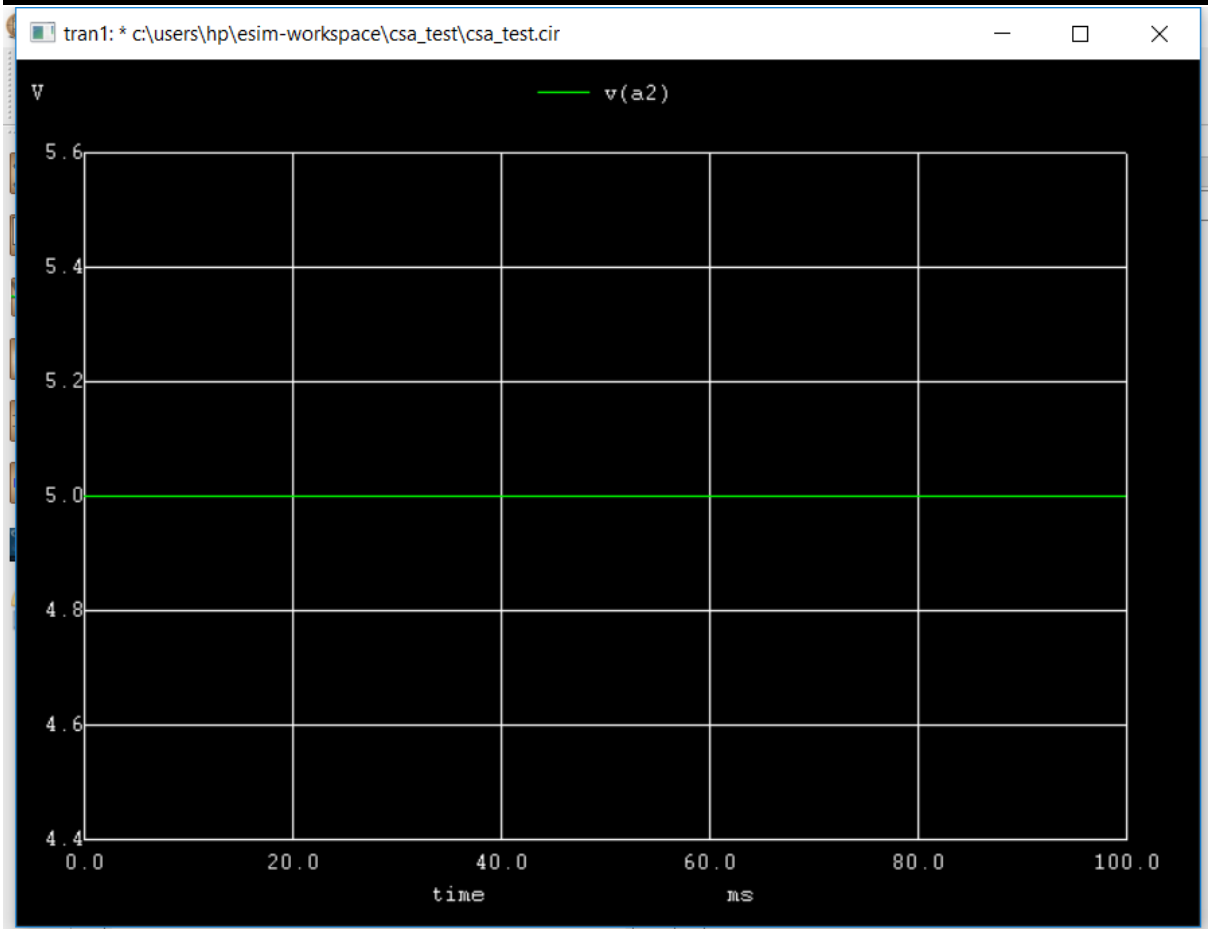
Here I used a subcircuit for four bit carry save adder.The internal structure of carry save adder is shown below.



Input Ngspice Plots:




tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(a1)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms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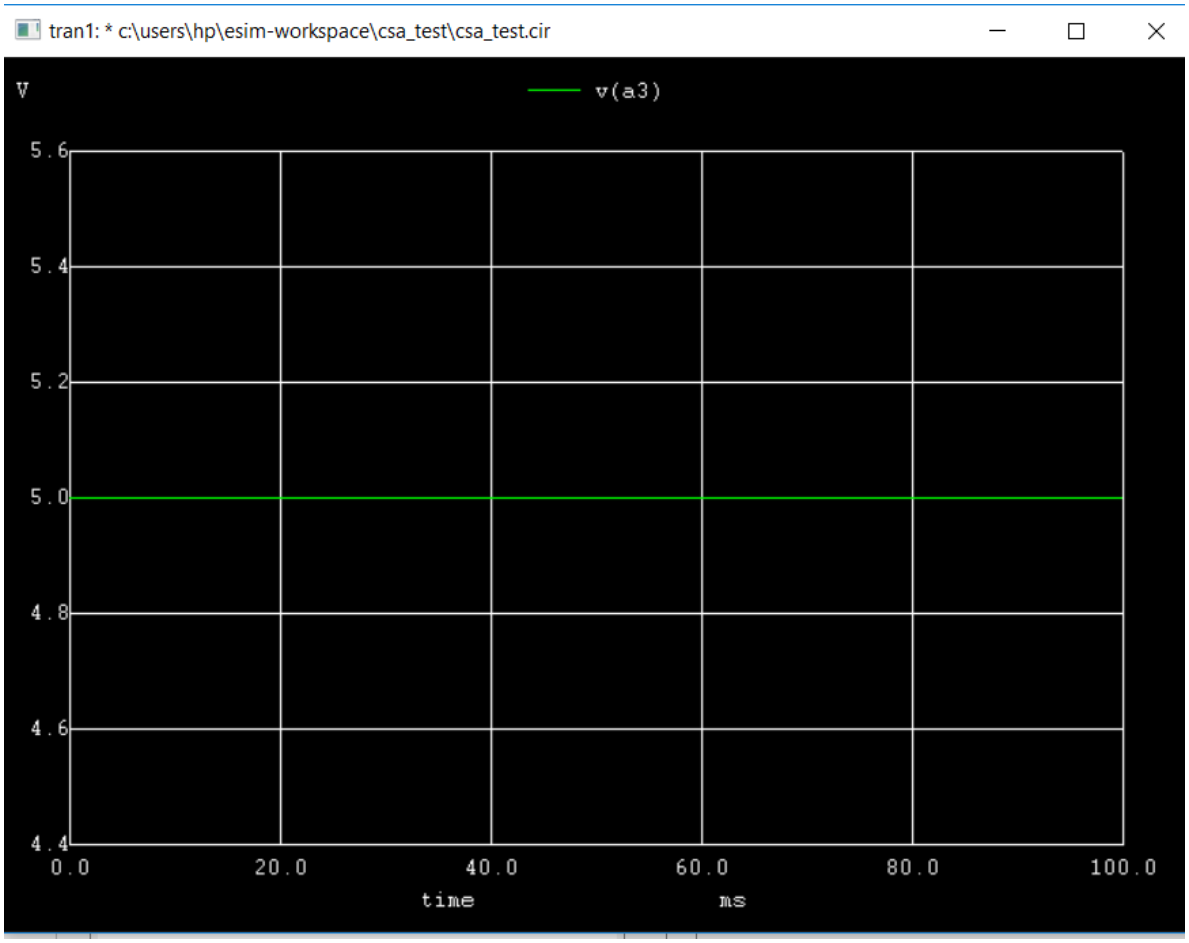
V
v(a2)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms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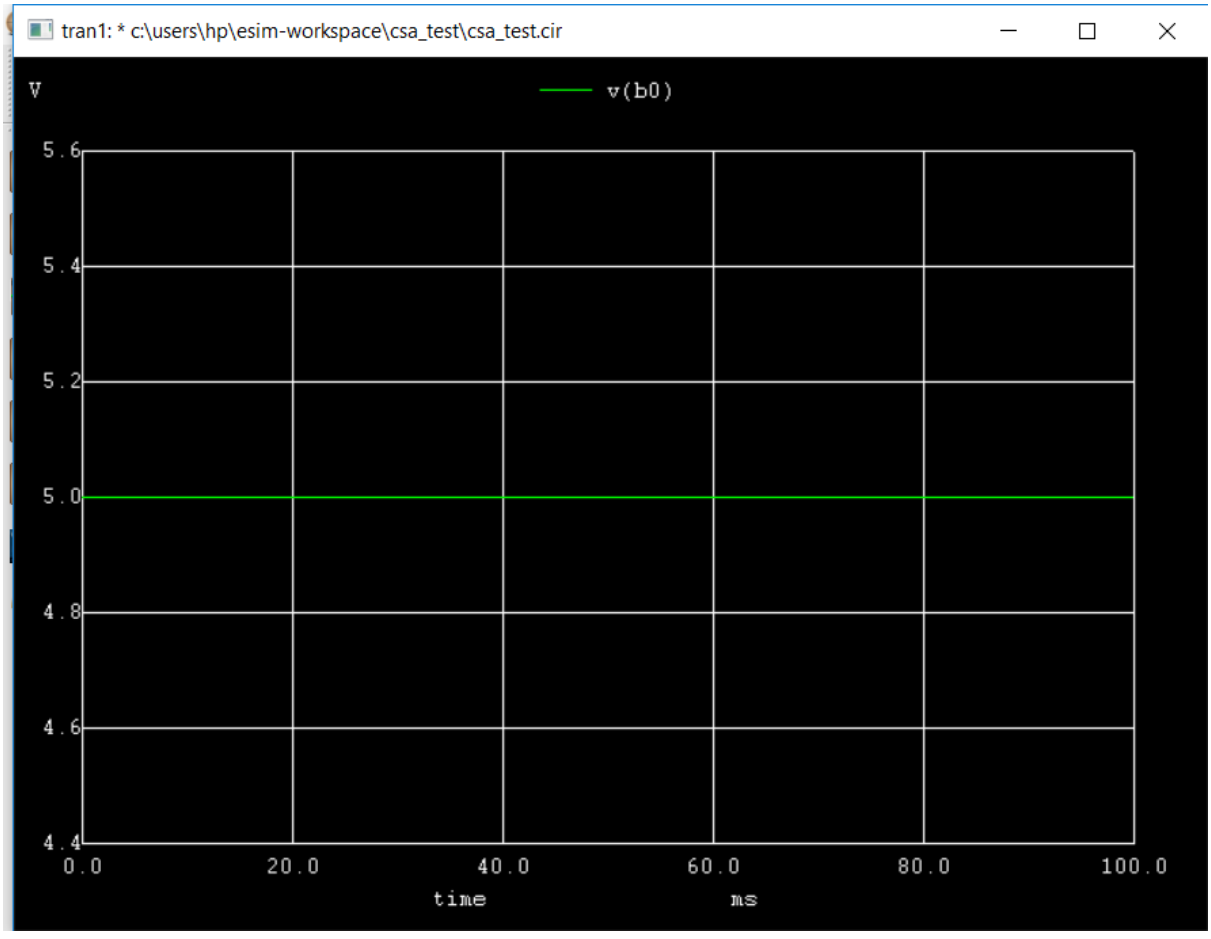
V
v(a3)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms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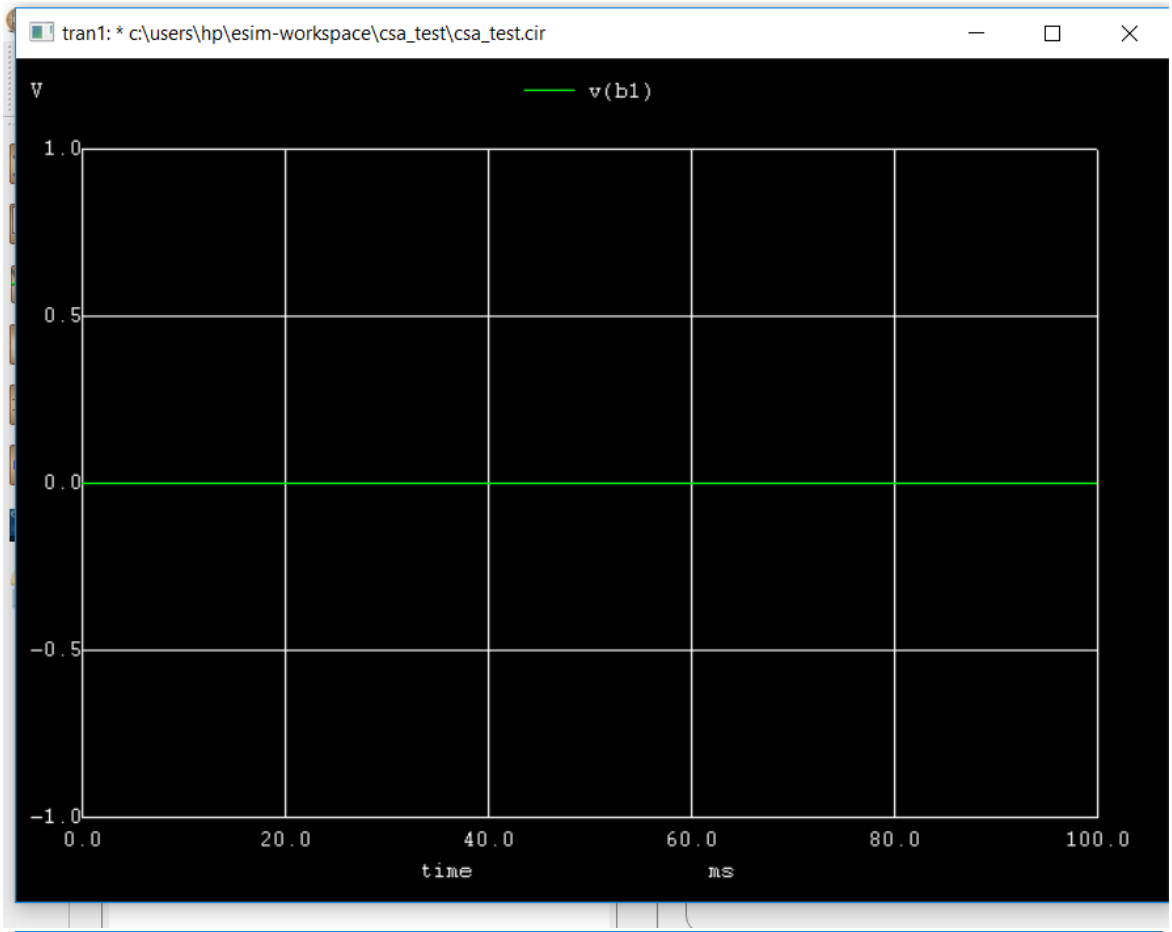
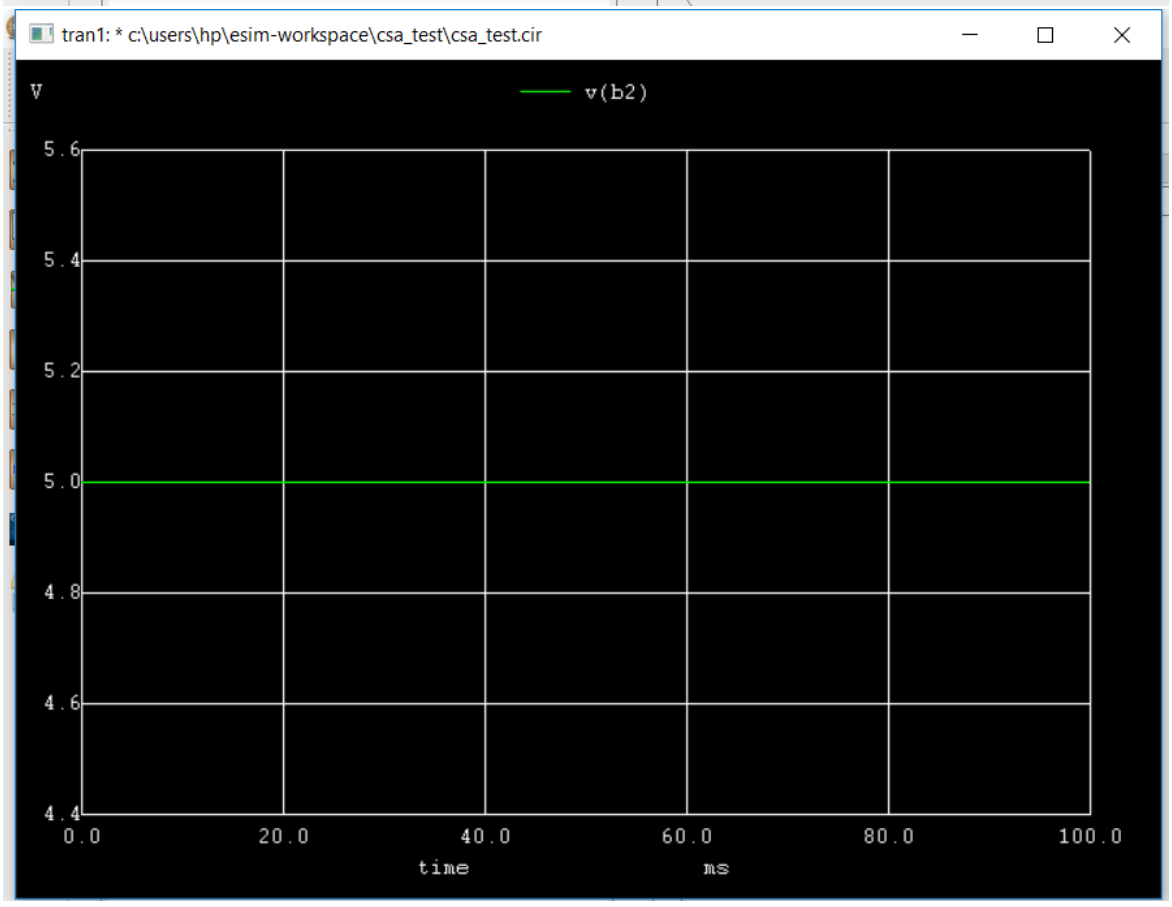
V
v(b0)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(b1)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms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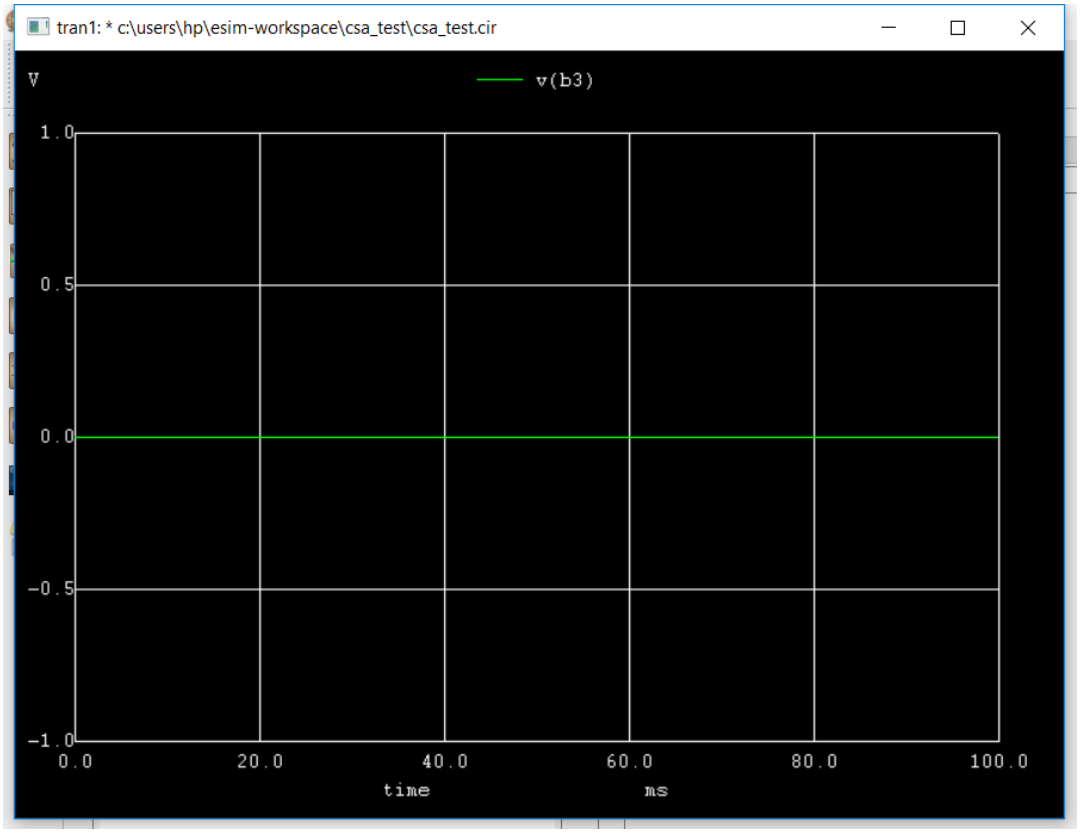
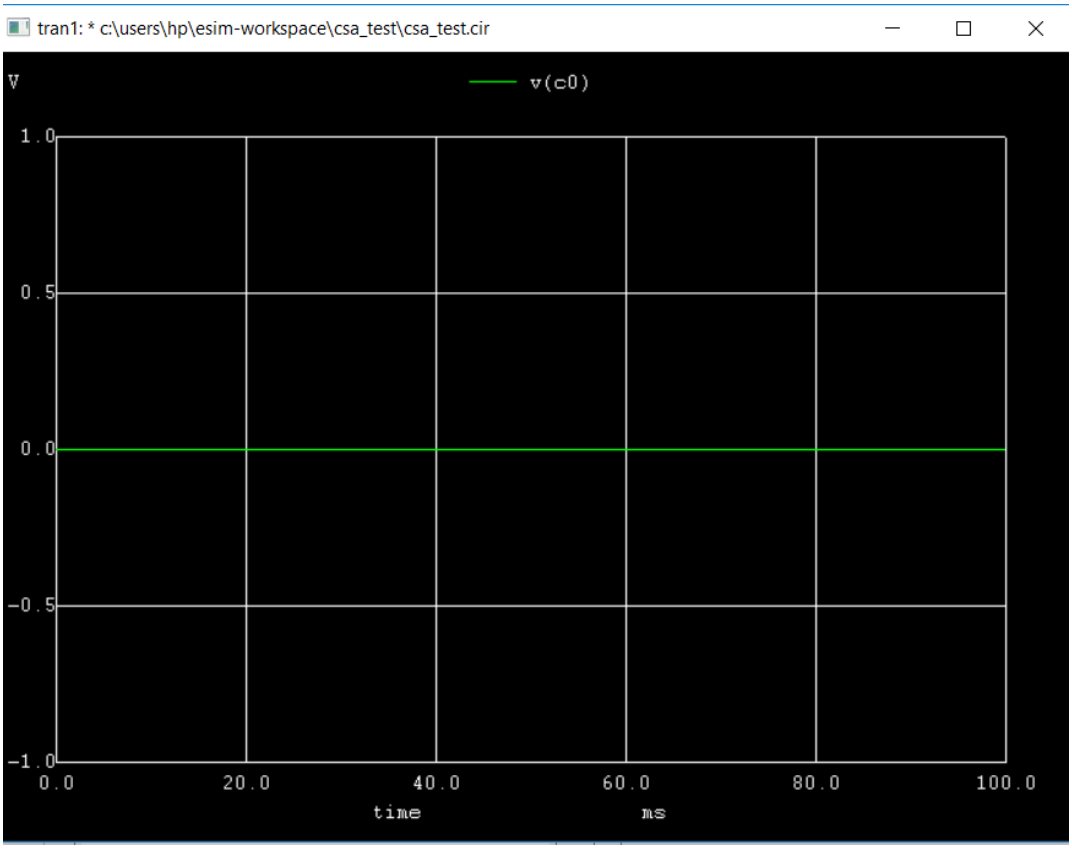
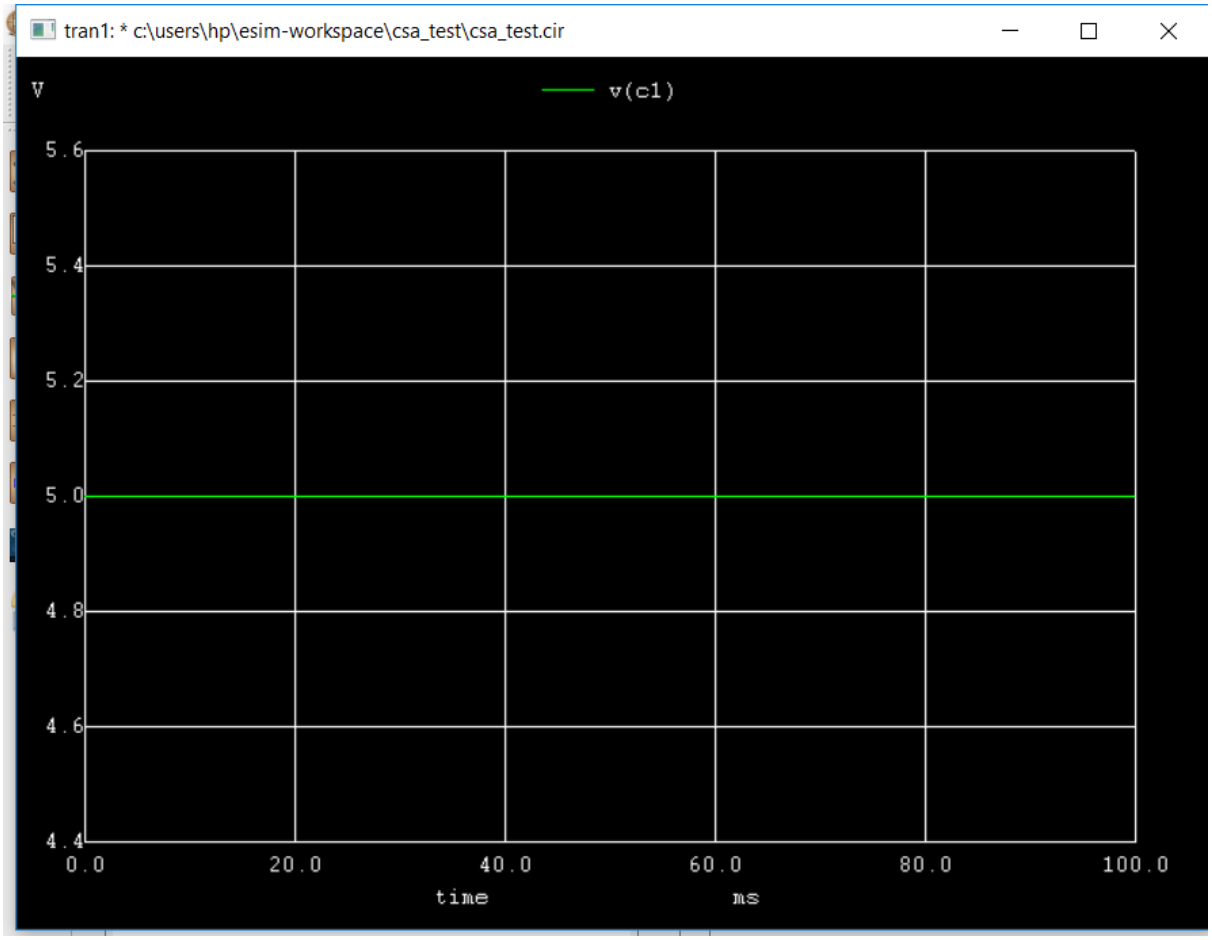
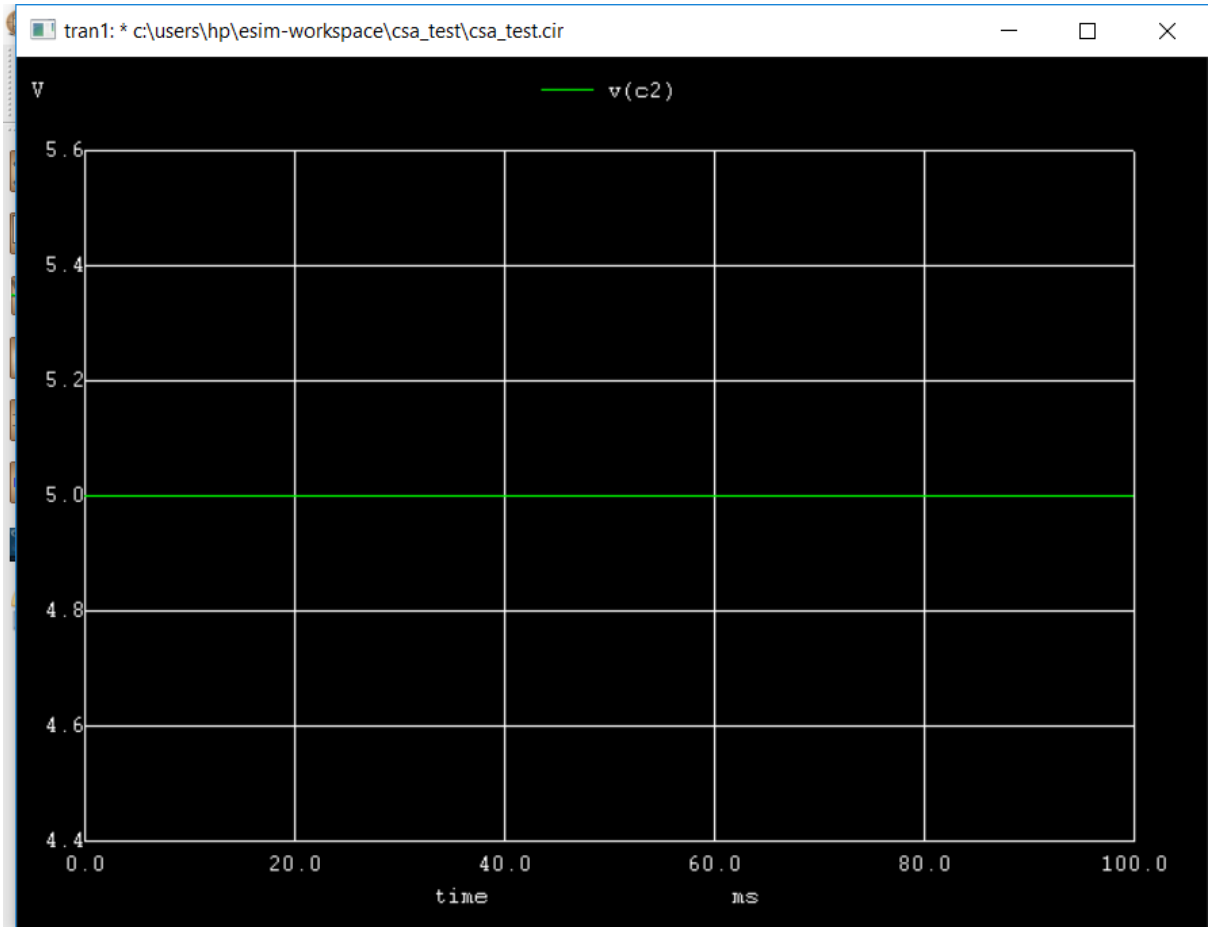
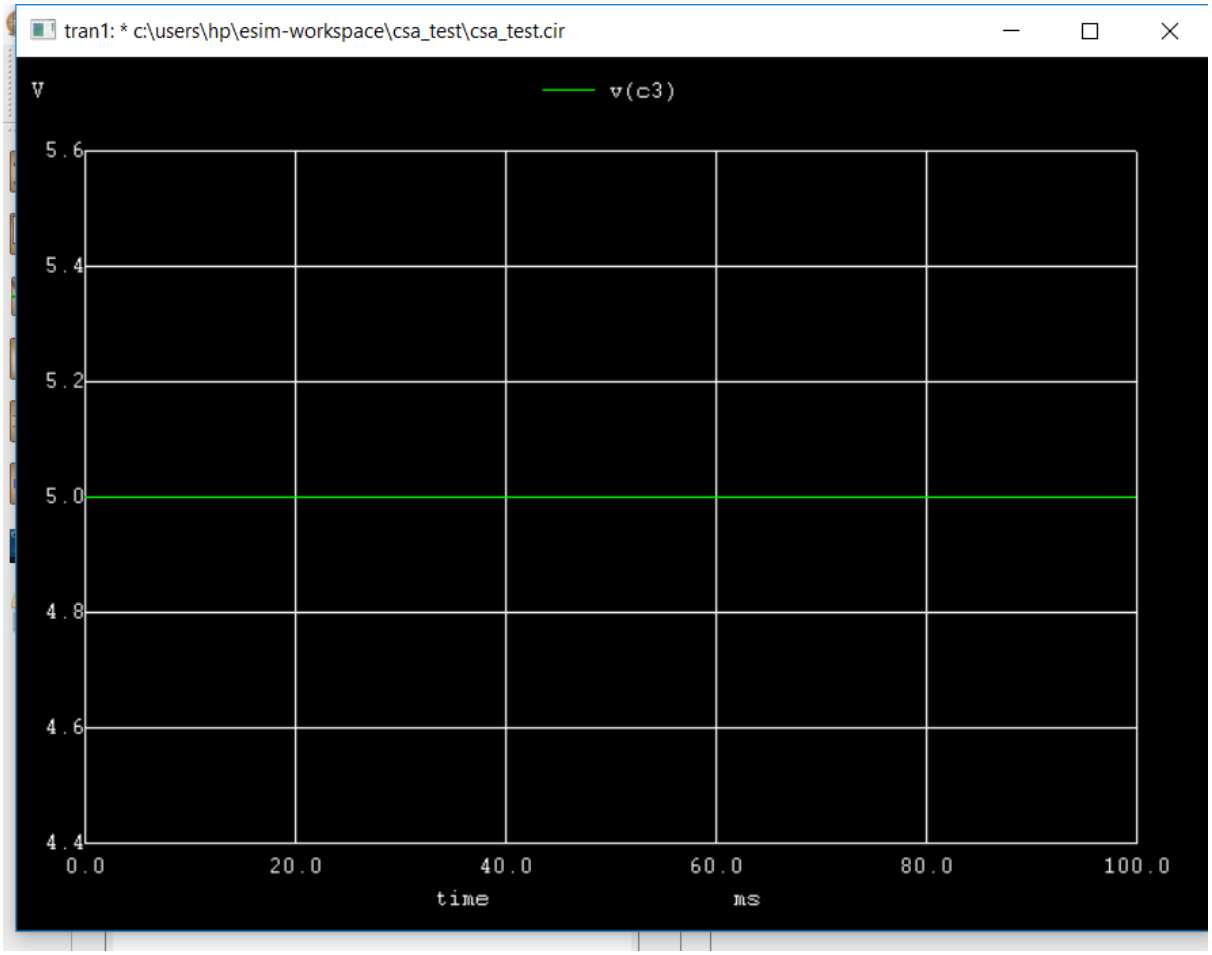
V
v(b2)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(b3)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

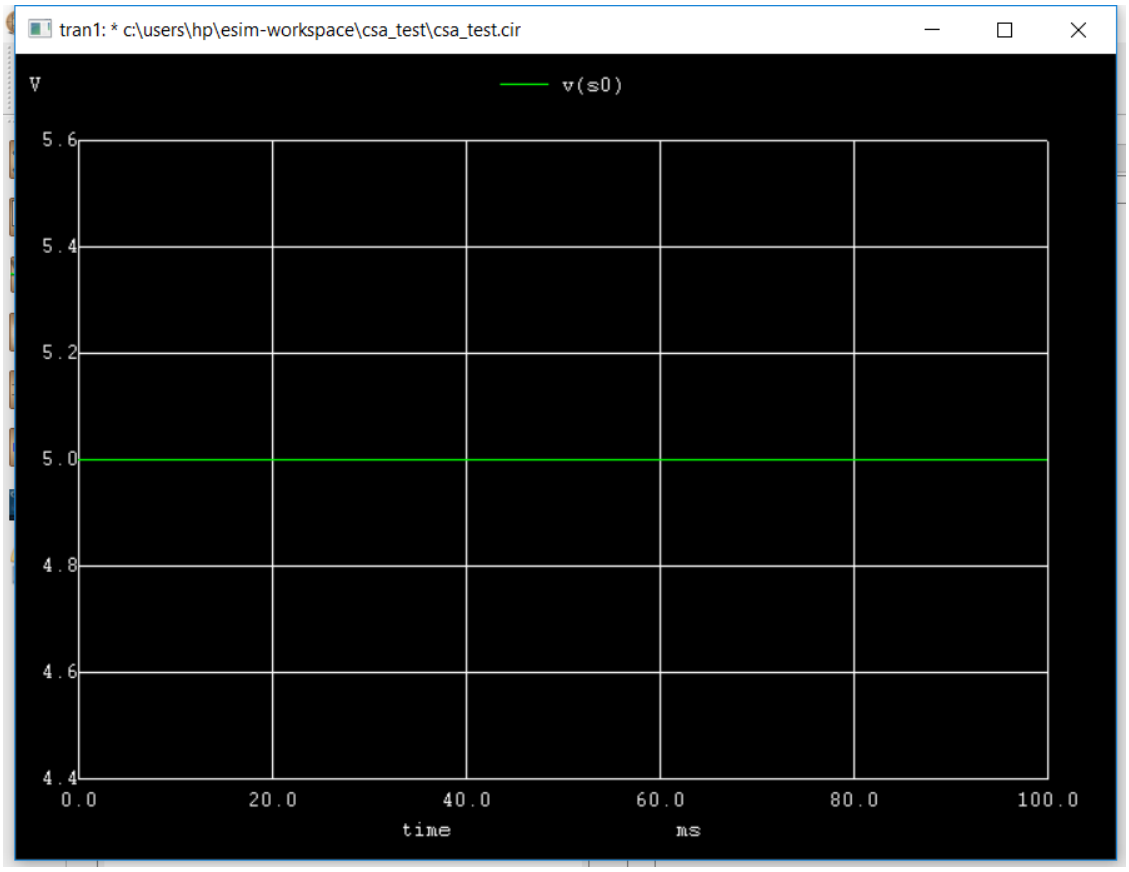

tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(c0)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

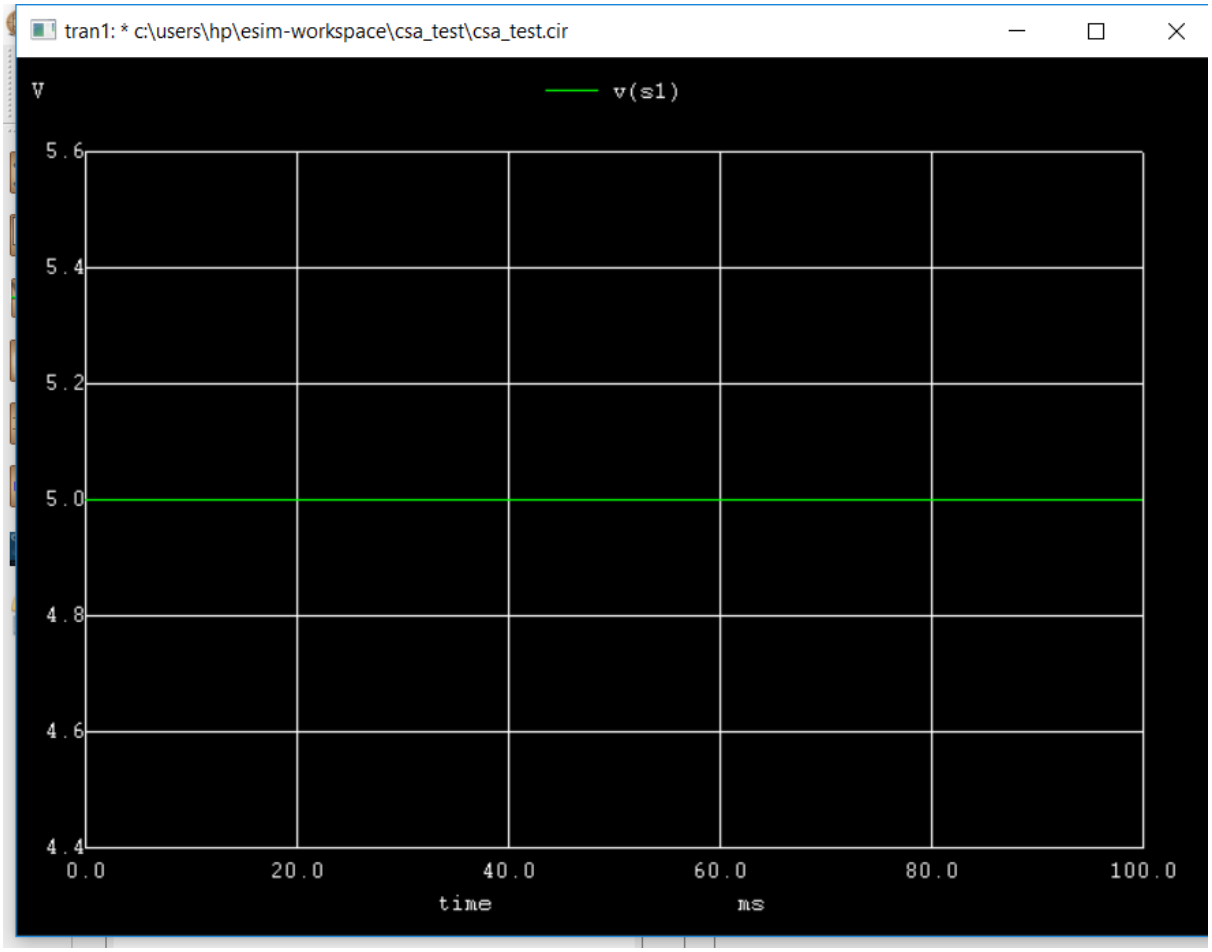

tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(c1)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

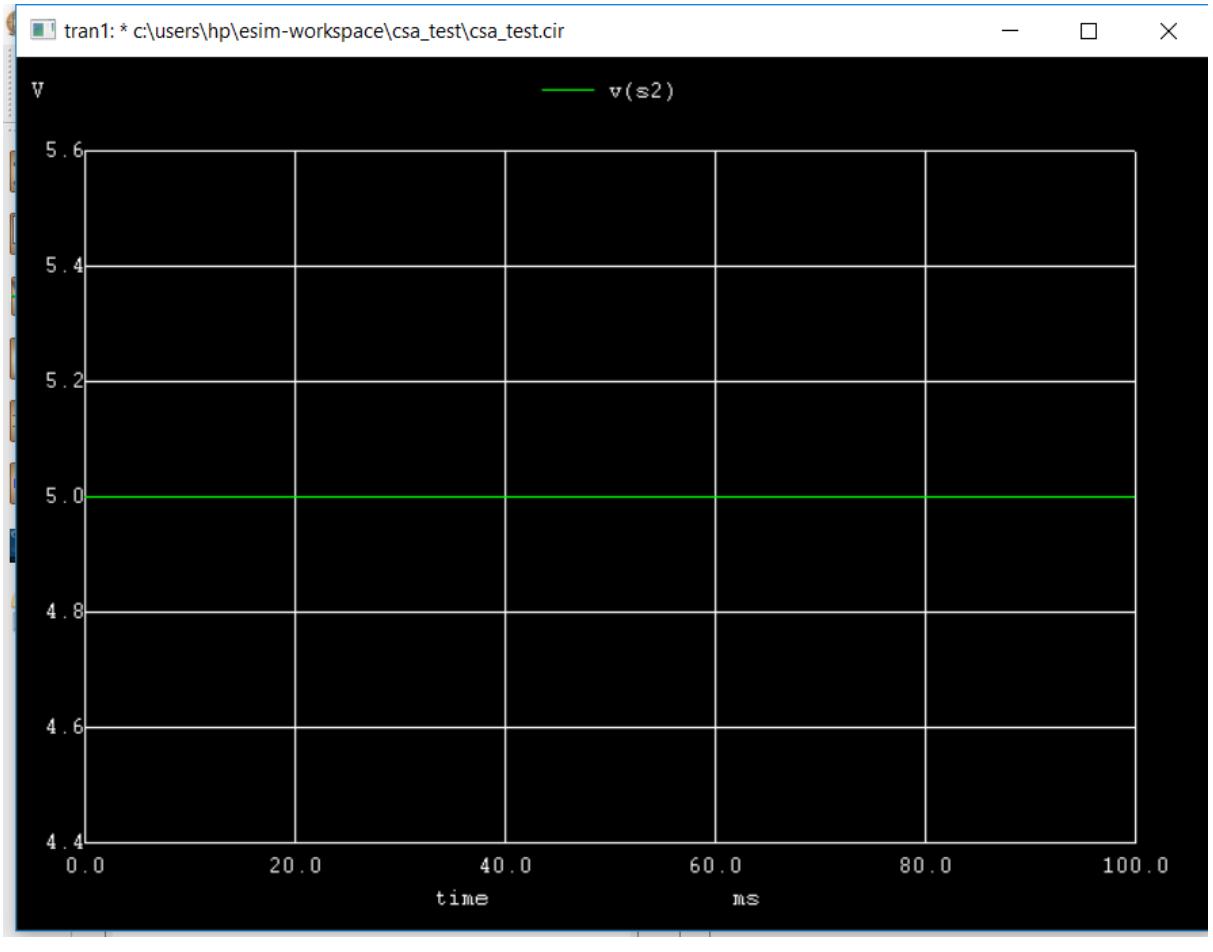

tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(c2)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

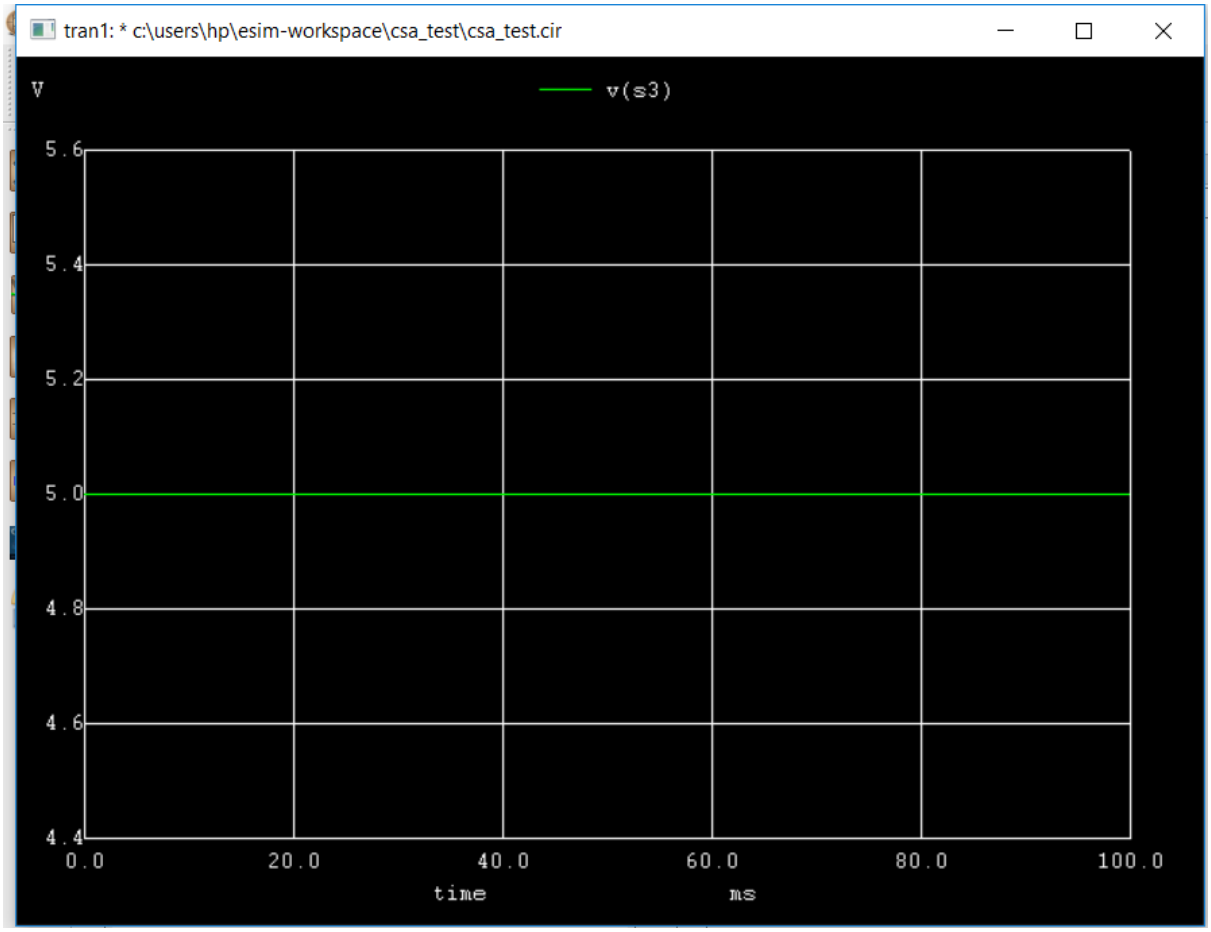


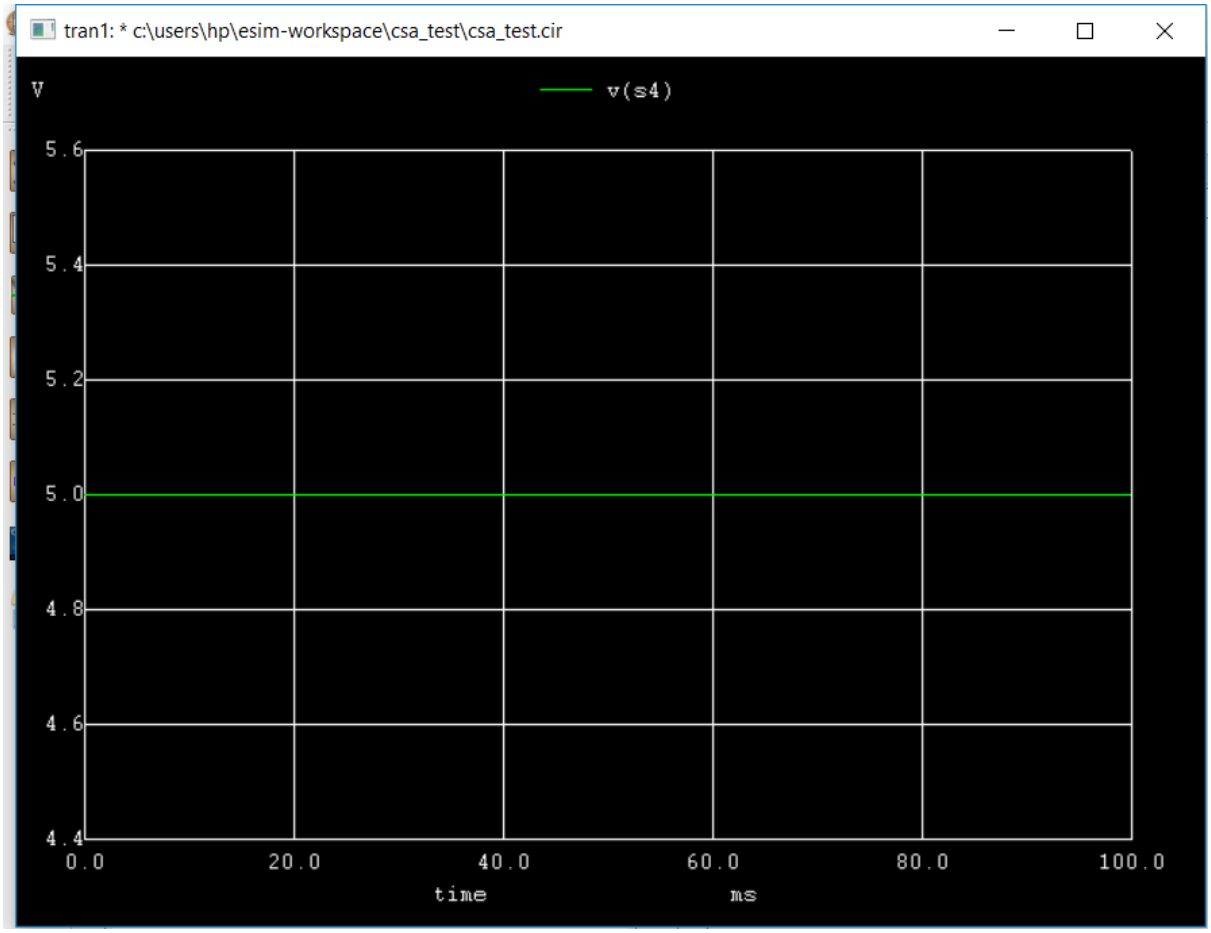
Output Ngspice Plots:

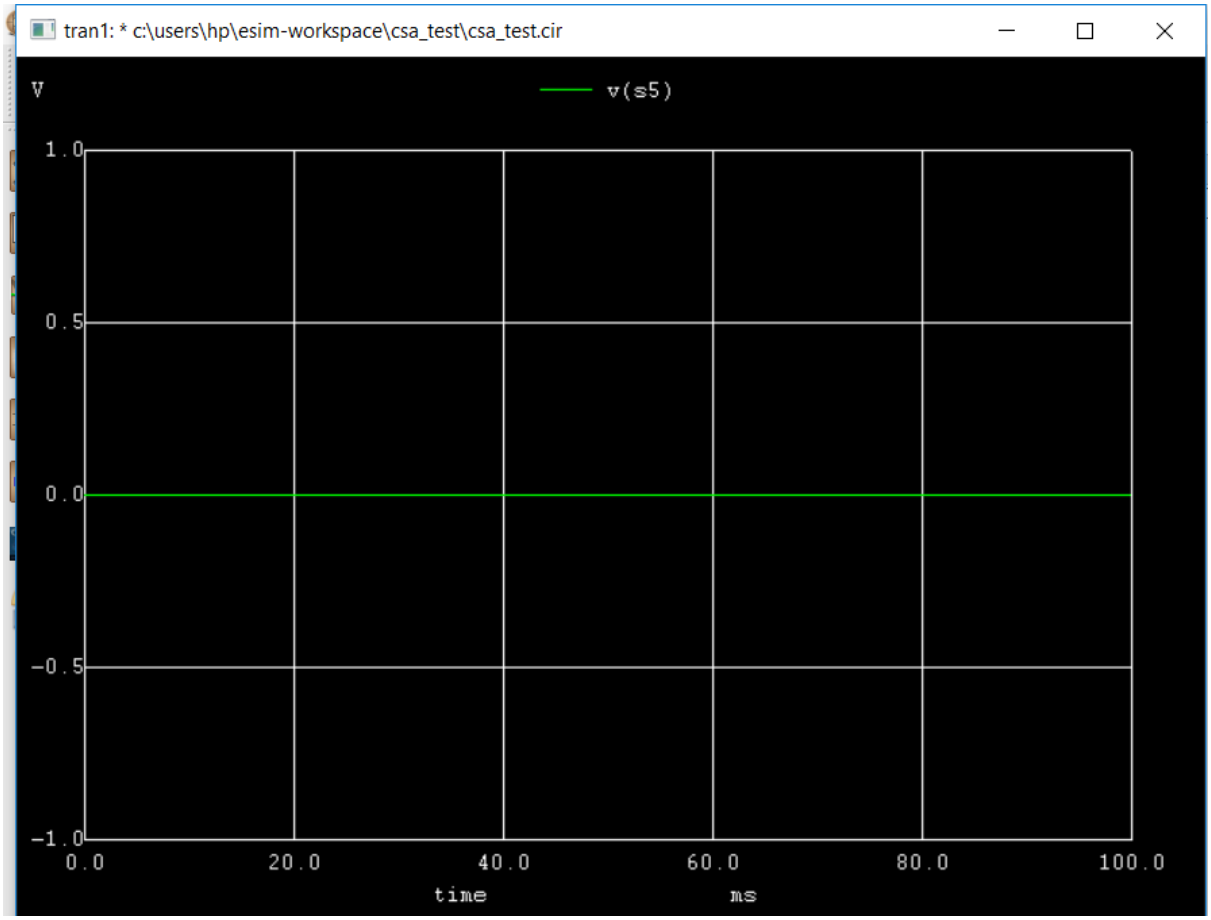



tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(s1)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

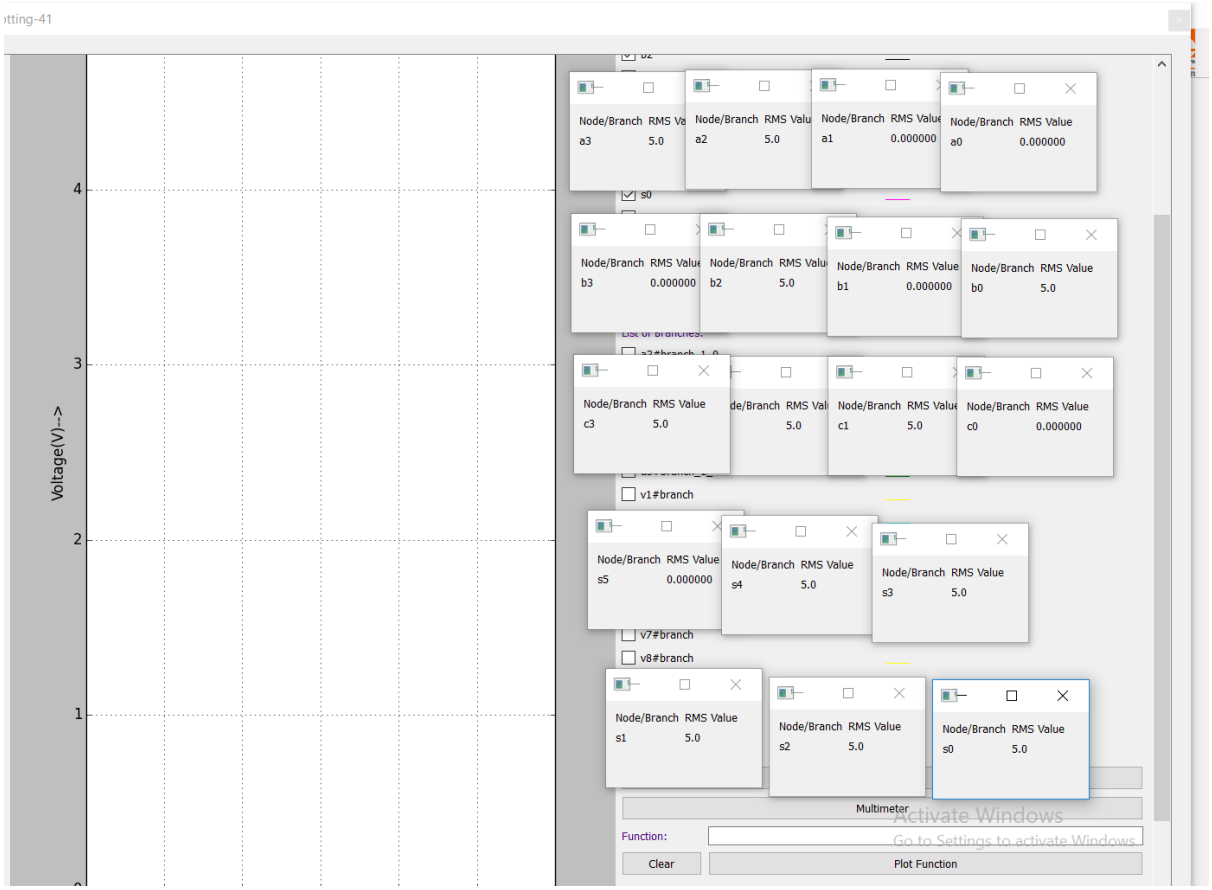

tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(s2)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(s3)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(s4)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\csa_test\csa_test.cir
V
v(s5)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Python Plot:



References:

https://www.researchgate.net/figure/4-bit-Carry-Save-Adder_fig2_322057640