RTL Inverter Gate Design and Simulation

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1 Theory:

In the digital circuit design various logic families are introduced in different time. Resistor Transistor Logic (RTL) family is one of the classical digital circuit design approach. In RTL design family, only resistors and bipolar junction transistors (BJTs) are used to design the various boolean functions. Behaviour of any inverter circuit is very simple, output goes to HIGH (logic '1') state when applied input signal state is LOW (logic '0') and for HIGH (logic '1') input signal, output goes to (LOW logic '0') state. For RTL inverter circuit, emitter is connected to the ground and collector is tied with the collector supply voltage (V_{cc}) through collector resistor R_c. Input voltage (V_i) represents logic levels, which is applied to the base of the BJT through base resistor R_b. For the LOW input signal, BJT goes to cut-off state and output of the circuit goes to HIGH state and voltage level of the output node almost equal to V_{cc}. For HIGH input signal, BJT goes to saturation state and output goes to LOW state where voltage level of output node is equal to the voltage drop across the collector-emitter voltage (V_{ce}). In this project, only inverter circuit is designed and transient analysis is done.

2 Schematic Diagram:

The schematic diagram of RTL Inverter in eSim is as shown below:

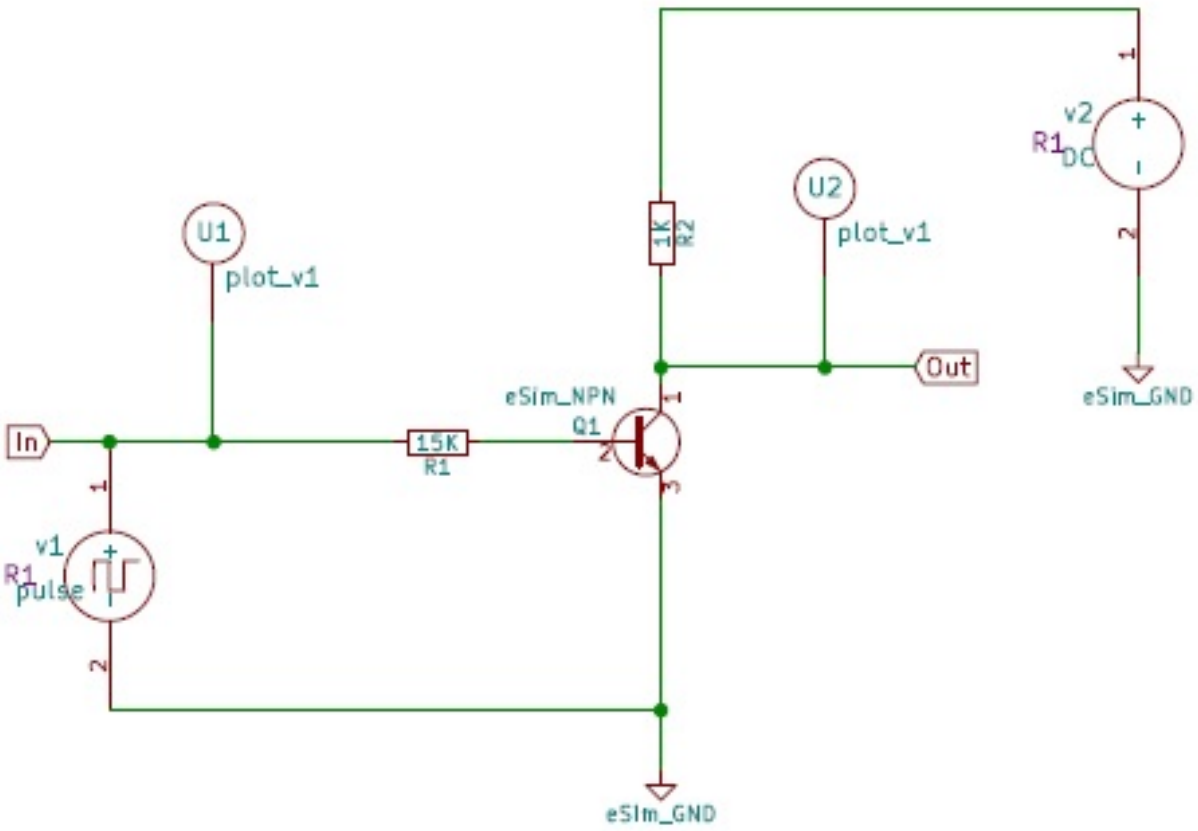

Figure 1: Schematic Diagram of RTL Inverter

3 Simulation Results

3.1 NgSpice Plots

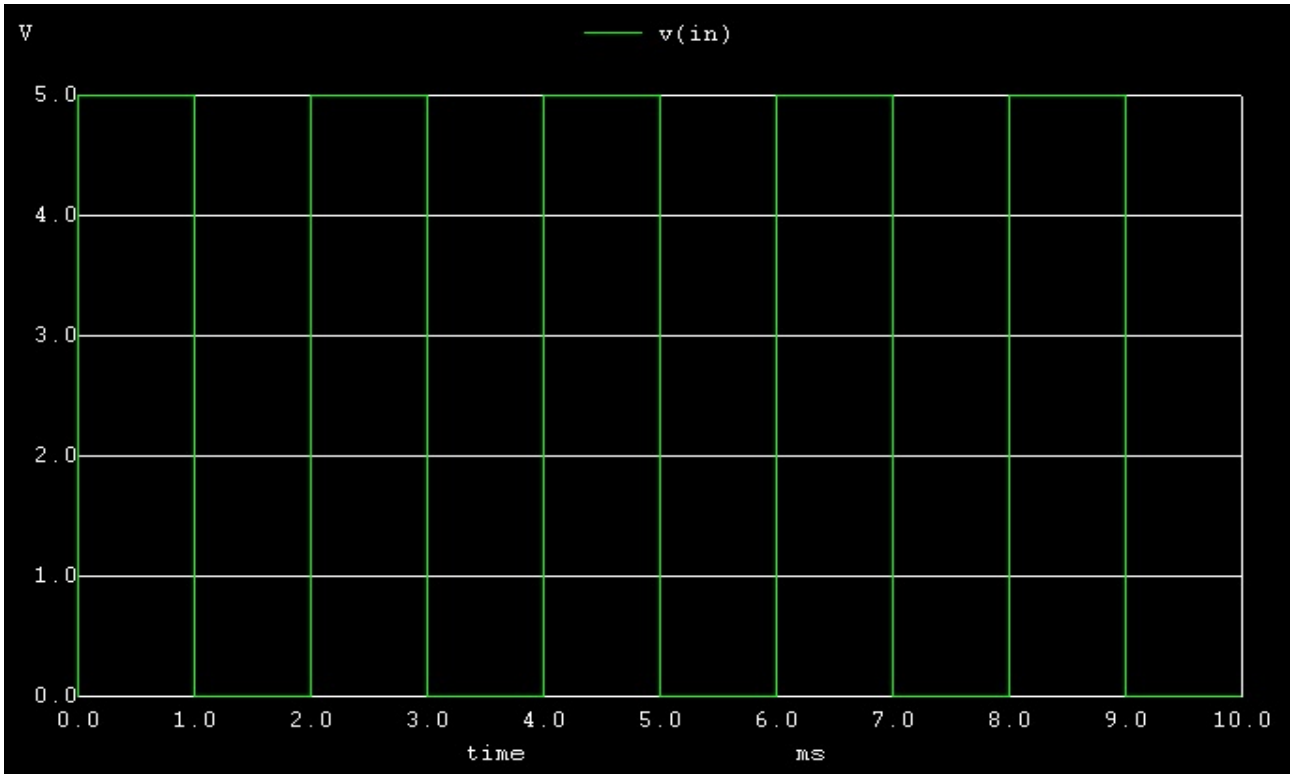

Figure 2: NgSpice Plot of Input Signal V(in)

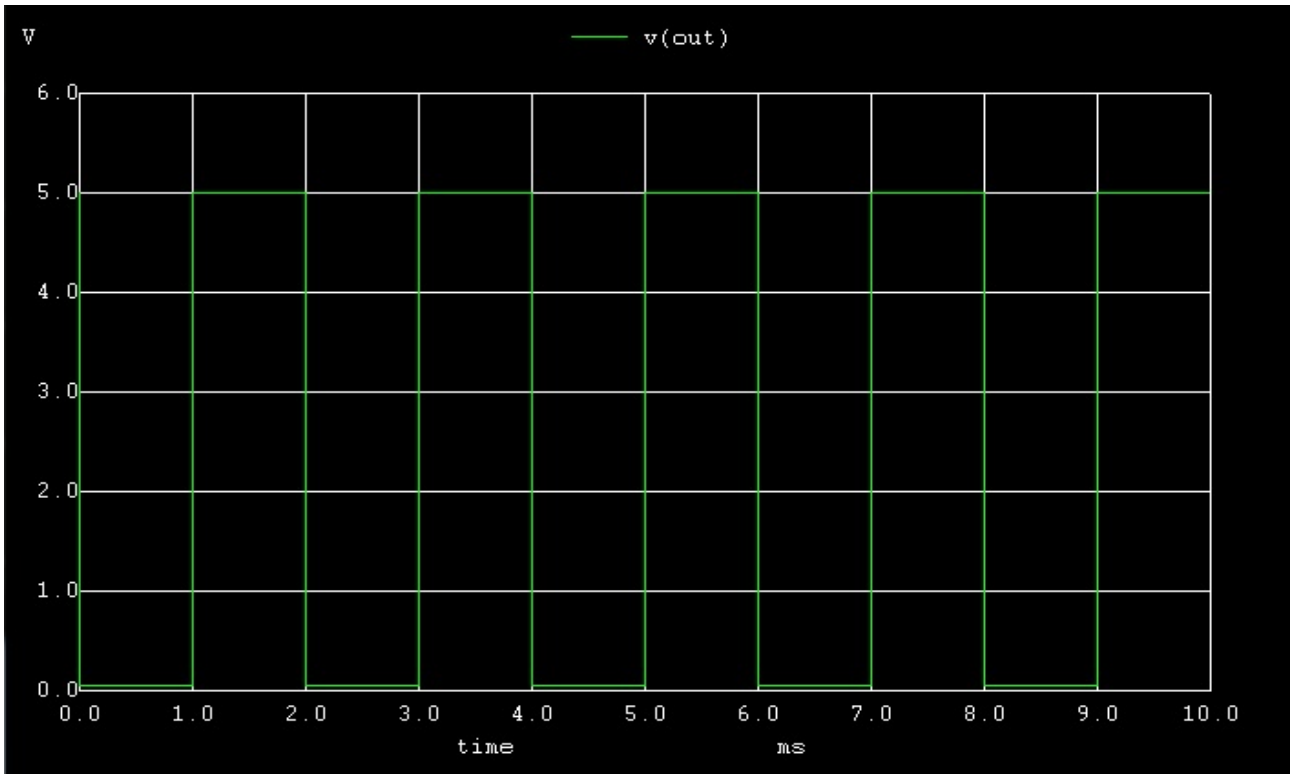

Figure 3: NgSpice Plot of Output Signal V(Out)

3.2 Python Plots

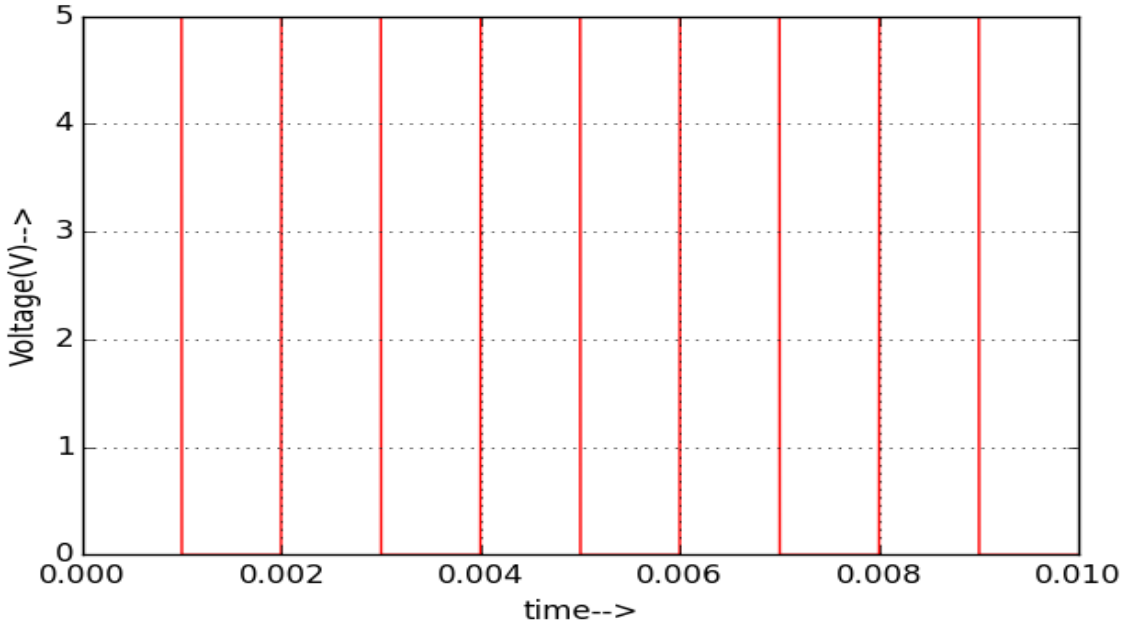

Figure 4: Python Plot of Input Signal V(in)

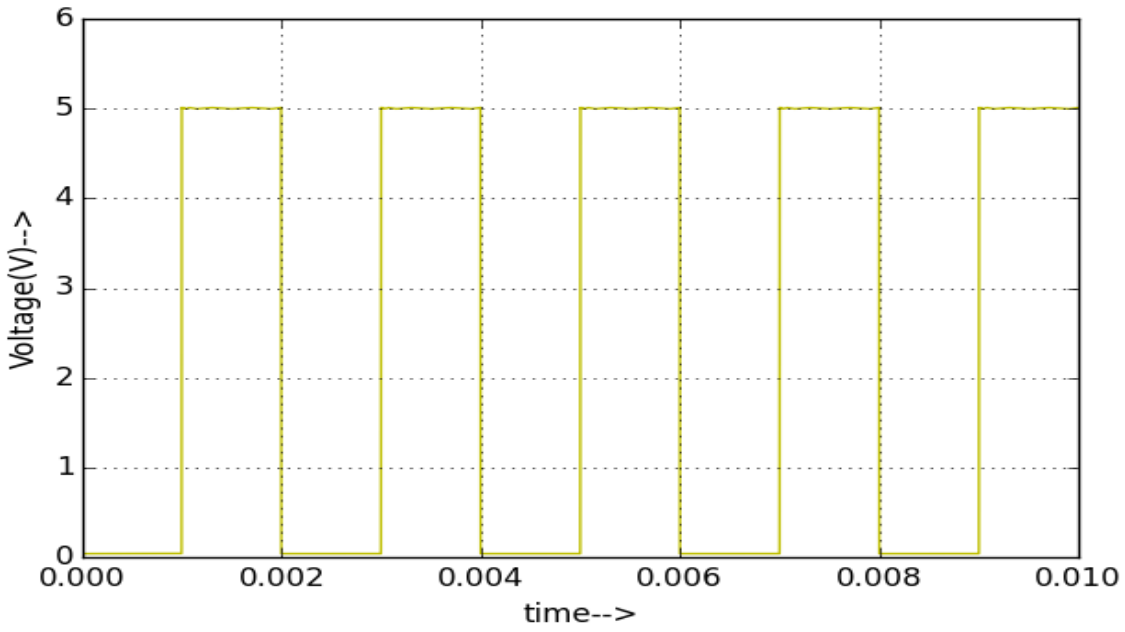

Figure 5: Python Plot of Output Signal V(Out)

4 Conclusion:

Thus, we have studied the transient response of the RTL inverter using eSim and we get the appropriate waveforms.

5 References:

http://www.play-hookey.com/digital_experiments/rtl/rtl_inverter.html