ABSTRACT

Carry Select Adder using BEC Logic

Athul M S , VIT Vellore

THEORY:

In the modern world of technology,people prefer to have gadgets with minimum size and maximum battery life. These demands can be met only through the application of high speed architectures. Carry Select Adder (CSA) is one such architecture where the carry propagation delay is reduced by generating multiple carries at the same time and then select a carry to generate the sum. However, due to the use of an extra Ripple Carry Adder (RCA) as the second stage and ultimately a final stage MUX the area consumed by such a CSA design is very huge, thus not only occupies a large area but also increases the power dissipation of the overall circuit, which can be a point of concern so as to make a device more and more portable. Hence in order to avoid the extra area and power consumption by the CSA, BEC Logic is used.

A BEC is a combination of XOR gates in conjugation with AND gates such that each and gate acts as an internal carry generator circuit that generates the carry of the two consecutive sum bits. The first sum bit S0 of the first stage RCA is passed through an inverter and inverted bit is taken as the first sum bit of add one operation. The first sum bit of first stage of RCA is ANDed with the second sum bit of first stage RCA, so as to generate the first internal carry bit. This carry bit generated is summed with third sum bit of the first stage RCA. The same process of generation of the carry from first stage sum bits and summation of consecutive internally generated carry bits with previous sum bits gives the overall add one operation using BEC logic. Thus we obtain the final sum bits for both the possibilities of carry being 0 by first stage RCA and carry being 1 by BEC logic block. These two sequences are sent to a final stage MUX array which selects any of the two sequences based on the previous stage carry being either 0 or 1.

CIRCUIT DIAGRAM :

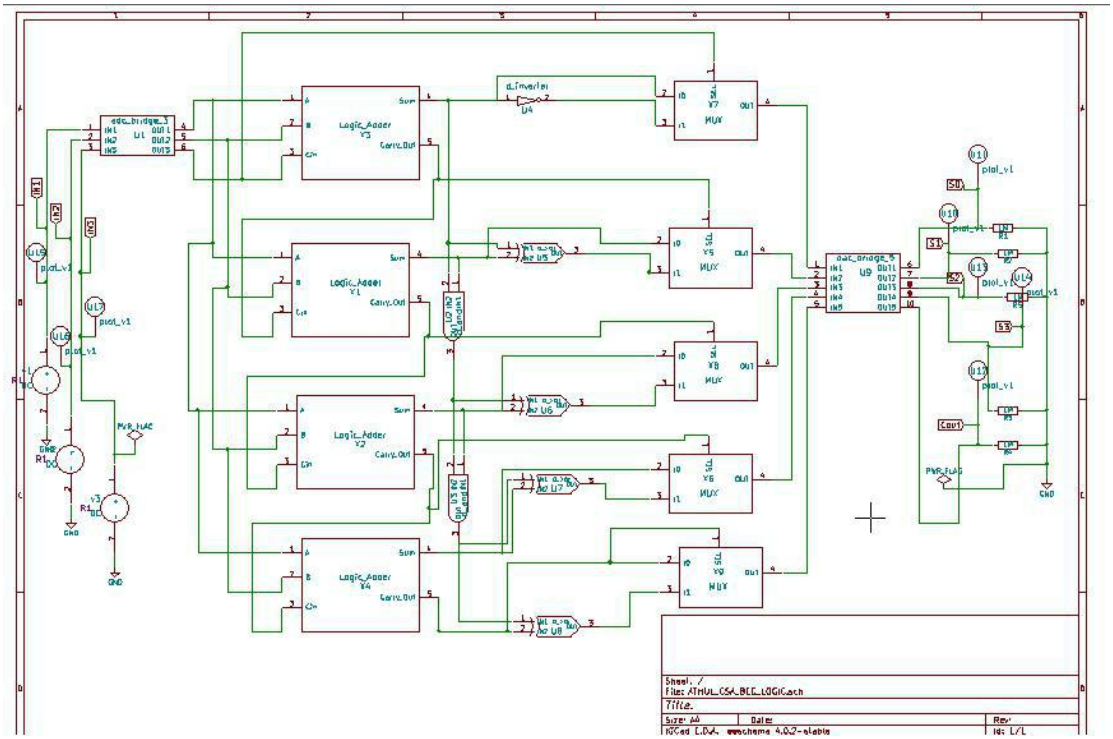

Fig.1 eSim Schematic of Carry Select Adder using BEC Logic

SIMULATION RESULTS :

1. Ngspice

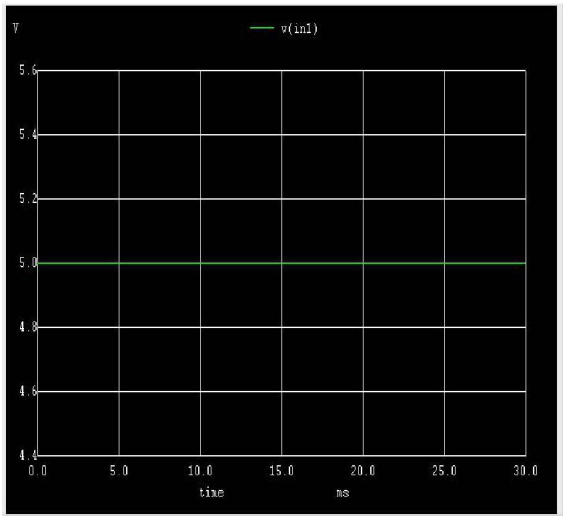

Fig.2 Input 1 DC Source = 5V; A0,A1,A2,A3=1

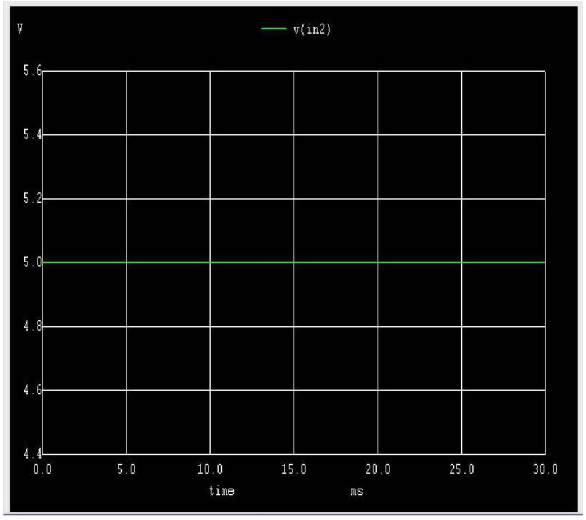

Fig.3 Input 2 DC Source = 5V; B0,B1,B2,B3=1

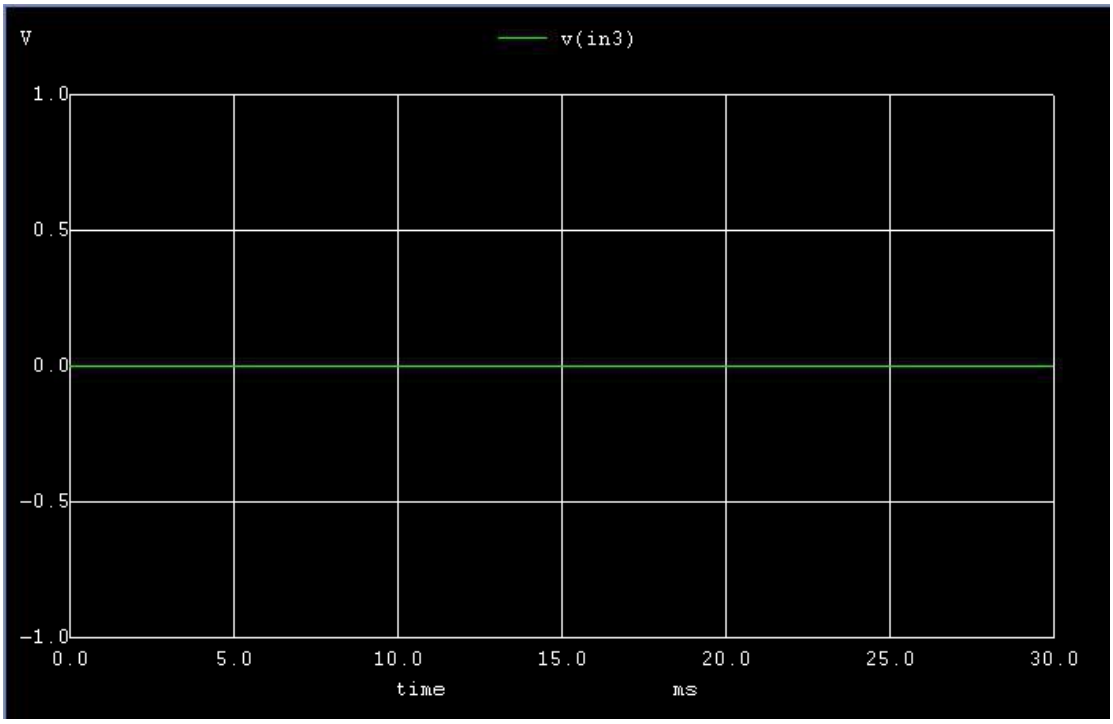

Fig.4 Input 3 DC source = 0V ; Cin=0

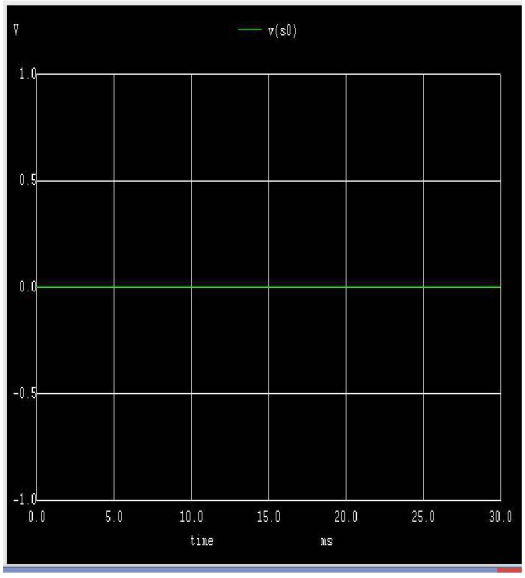

Fig.5 Output Sum;S0=0

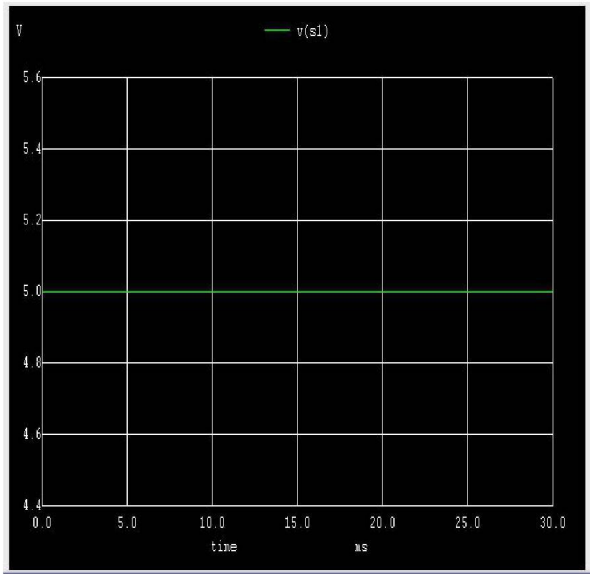

Fig.6 Output Sum;S1=1

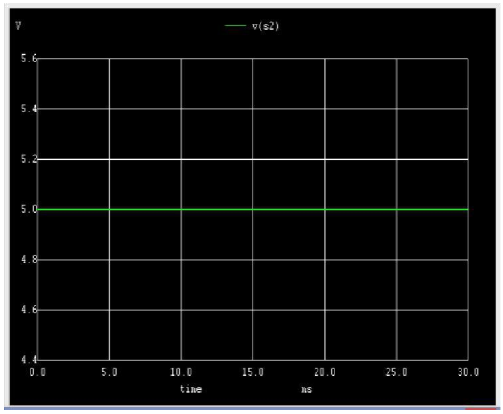

Fig.7 Output Sum;S2=1

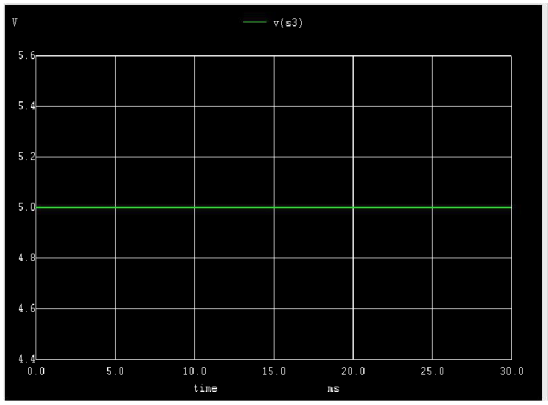

Fig.8 Output Sum;S3=1

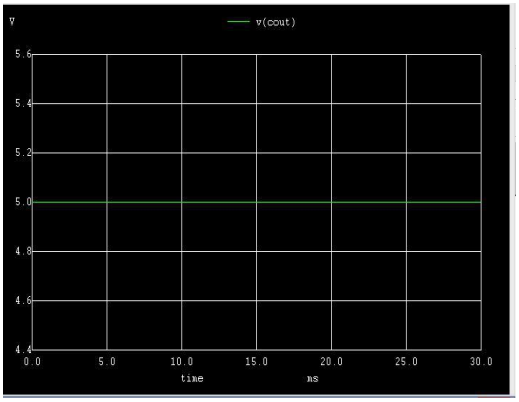

Fig.9
Output Carry;Cout=1

2.Python

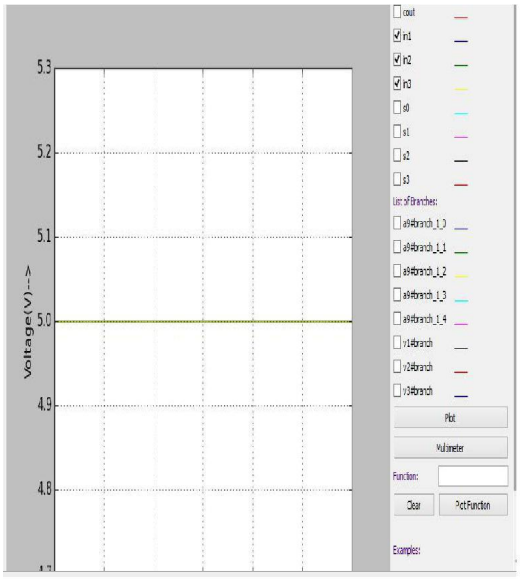

Fig.10 Inputs=1,Cin=0

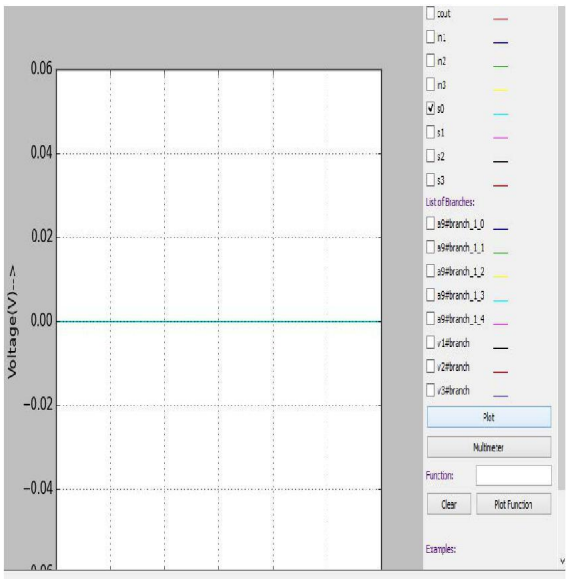

Fig.11 Output sum,s0=0

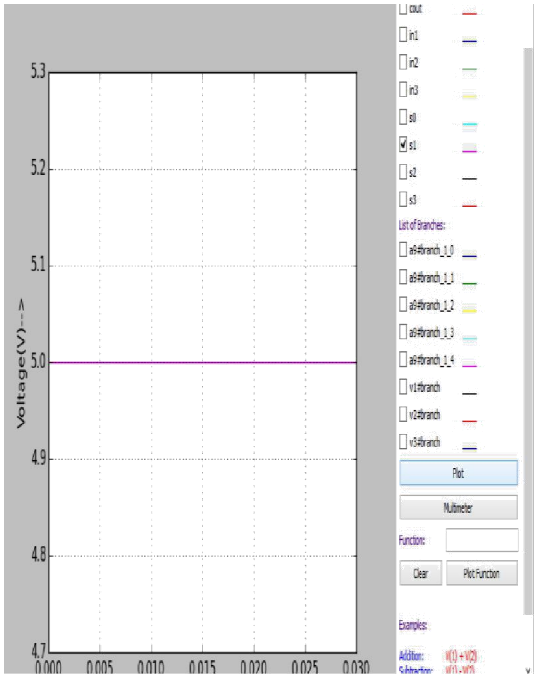

Fig.12 Output sum,s1=1

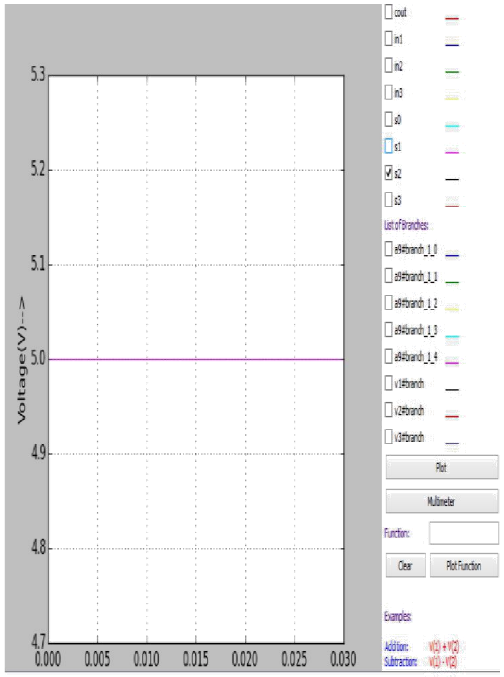

Fig.13 Output sum,s2=1

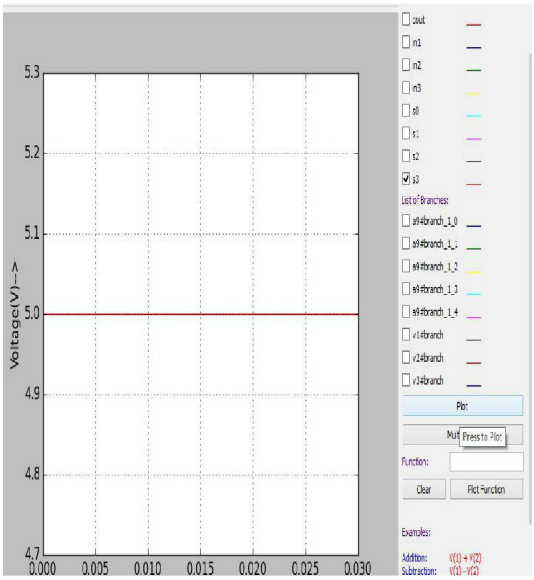

Fig.14 Output sum,s3=1

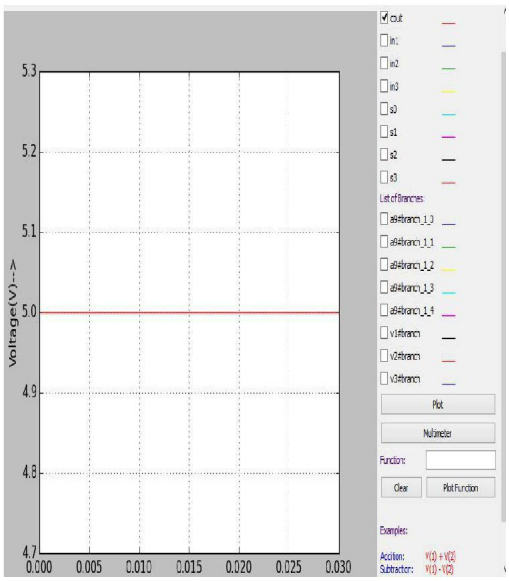

Fig.15 Output Carry,Cout=1

REFERENCES:

http://ieeexplore.ieee.org/document/7066706/